

Advanced Verilog HDL Design Techniques



Course Description

In this course, you will learn efficient coding techniques for writing synthesizable Verilog. You will gain experience in behavioral and structural coding while learning how to effectively write common logic functions including registered, memory and arithmetic functions. You will learn how to use Verilog constructs to parameterize your design, increasing their flexibility and reusability. While the concepts presented will mainly be targeting Altera® devices using the Quartus® II software, many can be applied to other synthesis tools as well. You will be introduced to testbenches and Verilog constructs used when building them. The hands-on exercises will use the Quartus II software to synthesize Verilog code and the ModelSim®-Altera tool for simulation.

Skills Developed

- Implementing synthesizable sequential and combinatorial RTL code
- Implementing finite state machines using multiple encoding schemes
- Debugging RTL code for common errors
- Developing simple testbenches for verification
- Using the Quartus II software to synthesis and verify results
- Running functional simulations in the ModelSim-Altera software

Prerequisites

We recommend completing the following courses:

- Introduction to Verilog HDL
- Verilog HDL Basics

Skills Required

- Completion of the "Introduction to Verilog HDL" course or some prior knowledge and use of Verilog hardware description language (HDL)
- Background in digital logic design
- Understanding of synthesis and simulation processes

Course Length	1 day
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

Exercises

- How to use IF-ELSE efficiently
- Create a 16-bit up/down counter with a modulus
- State Machine Encoding
- Operator Balancing, Resource Sharing & Pipelining
- Create a testbench to simulate a multiplier design
- Create a self checking testbench to simulate a multiplier design
- Writing Parameterized Code

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