

# Quartus II Design Series Foundation



## Course Description

You will learn how to use the Quartus® II software to develop an FPGA or CPLD. You will create a new project, enter in new or existing design files, and compile your design. You will also learn about timing constraints and analyze a design compiled with these constraints using the TimeQuest timing analyzer, the path-based static timing analysis tool included with the Quartus II software. You will learn techniques to help you plan your design. You will employ Quartus II features that can help you achieve design goals faster. You will also learn how to plan and manage I/O assignments for your target device.

## Skills Developed

- Make pre-project decisions to plan design
- Create, manage & compile Quartus II projects
- Plan & manage device I/O assignments using Pin Planner
- Assign clock & I/O constraints to improve design performance
- Analyze clock & input/output timing using TimeQuest
- Review compilation results

## Skills Required

- Background in digital logic design
- Ability to describe a hardware system using VHDL, Verilog or EDA schematic tool
- Experience with PCs and the Windows operating system

Course Length	1 day
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

## Exercises

- Create a project using the New Project Wizard
- Create a multiplier and RAM block using the MegaWizard Plug-in Manager to complete the design
- Create a HEX file to initialize the RAM block using the Memory Editor
- Analyze and elaborate the design to check for errors
- Perform full compilation
- Locate information in the Compilation Report
- Create a new revision to store new constraint settings
- Make design constraints using the Assignment Editor
- Assign I/O pins and perform I/O Assignment Analysis
- Use the Pin Migration View to see the effect of device migration on I/O assignments
- Create a clock constraint to complete an SDC file
- Follow the TimeQuest flow to generate timing reports
- Learn about using the TimeQuest interface

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