

# Quartus II Design Series Optimization



## Course Description

You will learn advanced features of the Quartus® II design software v.9.1 that will enable you to shorten your design cycle as well as improve your design performance and utilization. You will use the incremental compilation flow and LogicLock™ regions in the Quartus II software to reduce compile times and preserve performance on selected regions of your designs. You will obtain your design goals in the area of performance, resource usage and power consumption by using design strategies, HDL coding styles and Quartus II software settings. You will also learn how to manage compile times effectively.

## Skills Developed

- Define physical region constraints for an FPGA design using LogicLock regions
- Manage user-defined design partitions using the Quartus II incremental compilation flow
- Apply incremental compilation to the top-down & bottom-up design flows
- Use Quartus II software settings to improve internal & I/O timing, reduce logic resource usage & lower power consumption
- Choose recommended HDL coding styles
- Run Design Space Explorer to select optimal setting for full or partial designs

## Prerequisites

We recommend completing the following courses:

- The Quartus II Software Design Series: Foundation (Instructor-led Training)
- The Quartus II Software Design Series: Foundation (Online Training)
- The Quartus II Software Design Series: Timing Analysis
- TimeQuest Timing Analyzer

Course Length	1 day
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

## Skills Required

- Experience with PCs and the Windows operating system
- Completion of "The Quartus II Software Design Series: Foundation" course OR a working knowledge of the Quartus II software
- Completion of "The Quartus II Software Design Series: Timing Analysis" course OR a working knowledge of Synopsys Design Constraints (SDC) and the TimeQuest timing analyzer

## Exercises

- Quartus II Incremental Compilation
- Timing Optimization
- Timing Optimization using PLLs

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