

# Quartus II Design Series Timing Analysis



## Course Description

You will learn how to constrain & analyze a design for timing using the TimeQuest timing analyzer in the Quartus® II software v. 9.1. This includes understanding FPGA timing parameters, writing Synopsis Design Constraint (SDC) files, generating various timing reports in the TimeQuest timing analyzer & applying this knowledge to an FPGA design. Besides learning the basic requirements to ensure that your design meets timing, you will see how the TimeQuest timing analyzer makes it easy to create timing constraints to help you meet those requirements.

## Skills Developed

- Understand the TimeQuest timing analyzer timing analysis design flow
- Apply basic and complex timing constraints to an FPGA design
- Analyze an FPGA design for timing using the TimeQuest timing analyzer
- Write and manipulate SDC files for analysis and controlling the Quartus II compilation

## Prerequisites

We recommend completing the following courses:

- The Quartus II Software Design Series: Foundation (Instructor-led Training)
- The Quartus II Software Design Series: Foundation (Online Training)

## Skills Required

- Experience with PCs and the Windows operating system
- Completion of "The Quartus II Software Design Series: Foundation" online or instructor-led course OR a working knowledge of the Quartus II software

Course Length	1 day
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	On request
Dates	On request

## Exercises

- Introduction to the TimeQuest Tool
- Clock Constraints
- Synchronous I/O Constraints
- Timing Exceptions & Analysis

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