

Quartus II Design Series Verification



Course Description

You will learn features of the Quartus® II software v. 9.1 that will enable you to verify your FPGA design*. You will learn how to simulate Altera IP and mega-functions in other EDA simulation tools and how to use NativeLink to simulate directly in the Quartus II software from 3rd-party tools. You will also estimate FPGA power consumption using tools found in the Quartus II software. You will use debugging tools available in the Quartus II software, such as the SignalTap® II embedded logic analyzer, In-System Sources & Probes, & the Logic Analyzer Interface. You will learn to select the correct tool to effectively debug your design. *Some (not all) features examined by this course apply to CPLD designs

Skills Developed

- Analyze power consumption with the PowerPlay power analyzer
- Debug designs in-system using the SignalTap II embedded logic analyzer
- Connect internal debug nodes to an external logic analyzer using the Logic Analyzer Interface
- View & edit embedded memory contents using the In-System Memory Content Editor
- Make incremental design changes with Chip Planner

Prerequisites

We recommend completing the following courses:

- The Quartus II Software Design Series: Foundation (Instructor-led Training)
- The Quartus II Software Design Series: Foundation (Online Training)

Skills Required

- Experience with PCs and the Windows operating system
- Completion of "The Quartus II Software Design Series: Foundation" course OR a working knowledge of the Quartus II software

Course Length	1 day
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Language	Presentation in German or English Slides and documentation in English
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Platform	PC Windows XP / Windows 7
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Pricing	On request
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Dates	On request
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Exercises

- Basic Simulation with ModelSim-Altera Starter Edition
- Simulating with Altera Megafunctions
- Power Analysis
- Debugging with In-System Sources & Probes and the SignalTap II Embedded Logic Analyzer

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