

# Altera® PCI Express® Design Workshop

**El Camino**  
Training - Engineering - Consultancy



## Description

Learn how to implement PCI Express (PCIe) protocols using Altera FPGAs. Optimize your design by taking advantage of the architecture, operating modes, and features discussed throughout the course. Gain an understanding of the fundamentals of PCIe protocol to interface to your application.

You will gain hands-on experience implementing PCIe solutions using the Quartus II MegaWizard. This course focuses on Stratix IV GX / GT PCI Express Hard IP blocks mainly. Differences to Cyclone IV GX and Arria II GX FPGAs are discussed. Special courses for Cyclone / Arria are options for in-house training.

## Skills Developed

- Learn the improvements of PCIe over PCI
- Describe PCIe basics and PCIe topology
- Describe the main PCIe characteristics and functionalities defined by the PCIe standards for Generation 1 and 2
- Understand the PCIe layered architecture
  - Transaction Layer
  - Data Link Layer
  - Physical Layer
- Utilize the PCIe user interface
  - Transactions and transaction layer packets
  - TLP requests and completion packets
  - Packet routing
- Software initialization and configuration
  - Configuration mechanisms, registers, and capabilities
  - Error checking and reporting
  - Power management
- Describe the Altera PCIe solutions in general
  - Hard IP vs. Soft IP solutions
- Describe the Altera PCIe block architecture and functionality
  - Endpoints and Root Complex
- Designing with the PCIe Hard IP block
  - Usage of the PCIe Compiler
  - Using the compiler results
- Describe the Altera PCIe design flows
- Utilize the Altera PCIe block user interface
- Integrate the serial transceiver into the user design
- Apply the knowledge to a PCIe example design
- Learn about the user's responsibilities to design your own PCIe hardware
- Perform a PCIe Core design
  - Generation

Course Length	3 days
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows XP / Windows 7
Pricing	Public 1500,- EUR/attendee In-House On Request
Dates	See schedule at <a href="http://www.elcamino.de">http://www.elcamino.de</a>

- Simulation
- Implementation
- Describe the board design requirements
  - Layout considerations
  - Mechanical design requirements and solutions
  - Electrical design requirements and solutions
- Learn how to use debugging options
- Apply the knowledge from this class in a real life lab using an Altera development kit plugged into a host system

## Skills Required

- Working knowledge of design entry and compilation using the Quartus II software
- Basic knowledge in PCI design is helpful
- Experience with PCs and the Windows operating system

## Exercises

- Transaction examples
- Generation of a PCIe core
- Integration of transceiver cores
- Simulation of a PCIe design
- Test physical link Endpoint - Host system

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