



Course Description

This three-day course is a general introduction to the SystemC class library and its use in system level design. You will gain a basic but complete understanding of SystemC, enabling you to create your own designs and to understand existing ones. In the hands-on laboratory sessions, you will put this knowledge to the test by writing simple but practical code. You will also learn the basic instructions needed for operating the simulation tools Incisive Unified Simulator (IUS) of Cadence or Modelsim of Mentor. Furthermore the implementation of test benches based on the SystemC verification library (SCV) will be covered.

Skills Developed

- Understanding the origin of the SystemC class library
- Using SystemC classes
 - Structural modeling devoted classes (modules, ports, channels and interfaces)
 - Behavioral modeling devoted classes (processes and events, the simulation kernel)
 - The SystemC simulation kernel flow control statements, tracing and debugging facilities
- The SystemC methodic
 - How to remodel SystemC channels at a different abstraction level (refinement)
 - How to create parametrized designs
- Understanding the SystemC verification library capabilities and usage
- Using commercial simulators (Cadence IUS or Mentor Modelsim) (possibly with mixed – language designs)

Course Length	3 days	
Language	Presentation in German or English Slides and documentation in English	
Platform	PC, Linux using the OSCI free implementation or one of the commercial simulators covered in the course	
Pricing	Public In-House	1500,- EUR/attendee On Request
Dates	See schedule at http://www.elcamino.de	

Skills Required

- Knowledge of the C++ programming language (you can refer yourself to the C++ Workshop that we offer if you should need a refresh)
- Prior, basic knowledge of a hardware description language such as VHDL or Verilog is a plus but is not mandatory
- No prior knowledge of Cadence IUS or ModelSim software is needed.

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