# Altera® Transceiver Design Workshop

El Camino
Training - Engineering - Consultancy

## Description

Learn how to implement high-speed I/O protocols using Altera serial transceivers. Optimize your design by taking advantage of the architecture, operating modes, and features discussed throughout the course. Gain an understanding of the fundamentals of signal integrity in high-speed design.
You will gain hands-on experience implementing high speed transceiver channels using the Quartus II MegaWizard Plug-In. This course focuses on Stratix IV GX / GT transceivers mainly. Differences to Cyclone IV GX and Arria II GX FPGAs are discussed. Special courses for Cyclone / Arria are options for in-house training.

## Skills Developed

- Understand basic transceiver functionality
- Describe transceiver block architecture in general
- Utilize transceiver clocking blocks and options
- Utilize transceiver PCS sublayer blocks and options
  - Phase compensation
  - Encoding
  - Word, Lane, and Clock Alignment
- Understand the blocks and options in PMA layer
- Describe the transceiver control functions
  - Resets, Power-down, Loopback
  - Calibration block
- Use the Transceiver MegaWizard Plug-In Manager
- Describe the transceiver design flow
- Implement and simulate a transceiver design
- Learn how to use Dynamic Reconfiguration
  - Basics
  - Examples
- Perform debugging transceivers
- Describe the power supply requirements and solution options
- Describe the signal interfacing requirements and solution options
  - Clock and signal interfacing
  - Signal integrity for transceiver board design
  - PCB trace design
- Apply the knowledge from this class in a real life lab using transceiver hardware

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| Course Length | 3 days |
| Language | Presentation in German or English<br>Slides and documentation in English |
| Platform | PC<br>Windows XP / Windows 7 |
| Pricing | Public 1500,- EUR/attendee<br>In-House On Request |
| Dates | See schedule at<br>http: //www.elcamino.de |

## Skills Required

- Working knowledge of design entry and compilation using the Quartus II software
- Basic knowledge in high-speed design is helpful
- Experience with PCs and the Windows operating system

## Exercises

- Encoding Example
- Clock Alignment
- Lane Alignment
- Transceiver design generation
- Transceiver design simulation
- Transceiver design implementation
- Dynamic reconfiguration
- Transceiver power estimation

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