

High Speed Analog II

Interface Board

User's Manual

Revision 1.0

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1. Introduction

This User's Manual is for the CEPD High Speed Analog II interface board (HSA-II). The HSA-II provides signal conditioning, analog-to-digital conversion, and digital-to-analog conversion, which allow users to experiment with Digital Signal Processing algorithms implemented in FPGAs or other devices.

We reserve the right to make changes without notice to the boards or specifications described in this document.

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Warning: This device may cause radio interference in the living area. The user may be required to carry out and be responsible for appropriate measures.

2. HSA-II Features

- 14-bit ADC; 125 MSPS.
- 14-bit DAC; up to 200 MSPS.
- 5th order Bessel filter from analog input to ADC.
- 5th order Bessel filter from DAC to analog output.
- Analog input and output connectors are SMB.
- Powered via 6 VDC input.
- Mates directly with CEPD's CAS10 and CXS200 and El Camino's Digilab 10K240 and 20K240 Development Boards.
- Option to mate with Avnet's Virtex-E and Virtex-II Development Boards.

3. Glossary

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
SMB	Connector used for analog signals
MSPS	Million Samples Per Second
Op-amp	Operational Amplifier
LPF	Low-pass filter

4. Board Description

This section gives a detailed hardware description of the HSA-II. Refer to the HSA-II schematic for this description.

4.1 Power

Separate digital (+3.3VDD) and analog (+3.3VA) power and grounds are used on the board. The input voltage to the linear regulators, using either the power jack or the two position terminal block, must be 6 volts DC. Diodes protect against reversed polarity on these inputs but no current limiting is included. A diode bridge allows the plug to the power jack to be either positive or negative tip. Negative analog power (-3.3VA) is used by the input op-amp to allow the analog input to be centered around ground. The +1.8VDD power is used for the digital supply voltage of the digital-to-analog converter (DAC).

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4.2 Analog Inputs

A SMB connector provides the analog input. The analog source must have an impedance of 50 ohms and a maximum peak-to-peak voltage of 500mV. A signal conditioning low-pass filter (LPF) is used in the analog input path. This LPF is a 5th order Bessel filter and has a default 3dB cutoff frequency at 12MHz. The filter cutoff frequency can be adjusted using the equations in section 5. The signal then passes through an op-amp circuit with a gain of 2 and a DC bias of +1.55V at the output. This provides a 1.0V peak-to-peak signal with the proper DC offset at the input pin to the ADC.

4.2.1 Analog-to-Digital Converter

A 14-bit, 125MSPS analog-to-digital converter (ADC), the ADS5500, is used to sample the input signal. The inverting input of the ADC is referenced to the common mode voltage output (+1.55V) of the ADC. This provides a DC offset that allows the input signal to swing 550mV above or below the bias voltage.

The output of the ADC is configured to use two's complement with the data valid on the falling edge of the clock. The voltage at the DFS pin can be adjusted by changing the values of R3 and R53 in order to use straight binary, the rising edge of the clock or both. See the ADS5500 Data Sheet for a description of ADC user options.

The conversion clock input comes from the on-board oscillator. The conversion clock input can be changed so that it comes from the host board if R26 is removed and R33 is placed.

Due to the internal logic of the ADS5500, there is a 16.5 clock cycle delay from input to output.

4.3 Analog Output

An op-amp converts the differential current outputs of the DAC to a single-ended signal. A signal conditioning low-pass filter (LPF) is used in the analog output path. This LPF is a 5th order Bessel filter and has a default 3dB cutoff frequency at 12MHz. The filter cutoff frequency can be adjusted using the equations in section 5. A SMB connector provides the analog output. The output should be AC coupled to remove the DC bias and should be terminated with a 50 ohm load.

4.3.1 Digital-to-Analog Converter

A 14-bit, 200 MSPS digital-to-analog (DAC) converter, the DAC5674, is used by the host to generate the output signal. The differential current outputs of the DAC range from 0mA to the full-scale current. The full scale current can be adjusted by changing the value of the resistor R40. A maximum full-scale current of 20mA is achieved by using a 2.0 Kilo-ohm resistor. The clock input to the DAC comes from the on-board oscillator. The clock input can be changed so that it comes from the host board if R32 is removed and R27 is placed.

4.4 Connectors

A 50-pin connector provides the interface to the host board. This connector directly connects to JP3 of the CAS10 and CXS200 and PA3 of the Digilab 10K240 and 20K240 development boards. See Table 1 for the default pin-out of J4. In order for the HSA-II to connect directly to Avnet's Virtex-E and Virtex-II development boards, several resistors must be removed and others placed. See Table 3 for a list of resistor values for each configuration. See Table 2 for the pin-out of J4 with the resistors changed for direct connection to various Avnet boards.

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In addition to the 50-pin connector, a two position terminal block and a power jack are provided for the DC voltage input. Standard SMB connectors, one for analog input and one for analog output, are also provided.

4.5 Power Supervisor

The on-board power supervisor circuitry is used to generate a reset signal to the ADC and DAC when the +3.3VDD power supply drops below 2.97V. A manual reset is generated if the host does not drive the nFPGA_RESET signal high.

5. Bessel Filter Component Calculations

The analog input and output filters are standard 5th order Bessel low-pass filters. Component values can be calculated for a given 3dB cutoff frequency, ω_0 , using the following formulae. R_0 is the termination and source impedance; C_1 , C_2 and C_3 are the shunt capacitors; L_1 and L_2 are the series inductors (these reference designators are only for the formulae and do not correspond to schematic components).

$$C_1 = (0.1743 / R_0\omega_0)$$

$$C_2 = (0.8040 / R_0\omega_0)$$

$$C_3 = (2.2582 / R_0\omega_0)$$

$$L_1 = (0.5072 R_0 / \omega_0)$$

$$L_2 = (1.1110 R_0 / \omega_0)$$

You must choose available component values as close as possible to the calculated values.

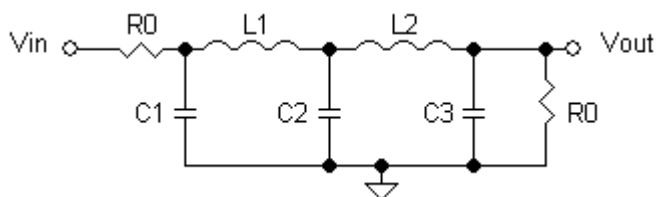


Figure 1 – Fifth Order Bessel LPF Configuration.

6. Tables

Table 1 – Host Connector, J4, Default			
<i>Signal Name</i>	<i>Pin #</i>	<i>Pin #</i>	<i>Signal Name</i>
DGND	1	2	NC
NC*	3	4	NC
NC	5	6	CLK
DACD2	7	8	DAC_PLLLOCK
DACD4	9	10	nFPGA_RESET
DACD6	11	12	DACD1
DACD8	13	14	DACD3
ADC_CLKOUT	15	16	DACD5
DGND	17	18	NC
ADC_OVR	19	20	DACD7
ADCD0	21	22	DACD9
ADCD2	23	24	DACD11
ADCD4	25	26	ADCD1
NC	27	28	NC
ADCD6	29	30	ADCD3
NC	31	32	ADCD5
DGND	33	34	NC
NC	35	36	ADCD7
ADCD8	37	38	ADCD9
ADCD10	39	40	ADCD11
ADCD12	41	42	ADCD13
DACD0	43	44	DACD13
DACD10	45	46	TP2
TP3*	47	48	DACD12
DGND	49	50	DGND

* NC = No Connect, TP = Test Point

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Table 2 – Host Connector, J4, Avnet			
<i>Signal Name</i>	<i>Pin #</i>	<i>Pin #</i>	<i>Signal Name</i>
DGND	1	2	nFPGA_RESET
DACD4	3	4	DACD1
DACD0	5	6	CLK
DACD2	7	8	DAC_PLLLOCK
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
ADC_CLKOUT	15	16	DACD5
DGND	17	18	DACD3
ADC_OVR	19	20	DACD7
ADCD0	21	22	DACD9
ADCD2	23	24	DACD11
ADCD4	25	26	ADCD1
DACD10	27	28	DACD13
ADCD6	29	30	ADCD3
DACD8	31	32	ADCD5
DGND	33	34	DACD12
DACD6	35	36	ADCD7
ADCD8	37	38	ADCD9
ADCD10	39	40	ADCD11
ADCD12	41	42	ADCD13
NC	43	44	NC
NC	45	46	TP2
TP3	47	48	NC
DGND	49	50	DGND
NC = No Connect, TP = Test Point			

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Table 3 – Resistor Values for Connection Options		
	22 Ohm	Do Not Place (DNP)
Default Connection	R66 R67 R68 R69 R70 R71 R86 R87 R88 R89	R60 R61 R62 R74 R80 R81 R82 R83 R84 R85
Avnet Connection	R60 R61 R62 R74 R80 R81 R82 R83 R84 R85	R66 R67 R68 R69 R70 R71 R86 R87 R88 R89

Attachments

The schematic diagram is attached.