

# High Speed Analog

## Interface Board

# User's Manual

## Revision 1.0

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## 1. Introduction

This User's Manual is for the HSA, High Speed Analog, interface board. This board connects to a Digilab 10Kx240 or 20Kx240 FPGA prototype development board. It may also be used with any host board that meets the connector pinout in Table 1. The HSA provides signal conditioning, analog-to-digital conversion, and digital-to-analog conversion, which allows users to experiment with Digital Signal Processing algorithms implemented in FPGAs.

We reserve the right to make changes without notice to the boards or specifications described in this document.

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*Warning: This device may cause radio interference in the living area. The user may be required to carry out and be responsible for appropriate measures.*

## 2. HSA Features

- Dual channel, 8-bit ADC; 40 MSPS;
- Single channel 8-bit DAC; up to 40 MHz operation;
- Analog DC, unbuffered, path directly to ADC;
- Analog 32 Hz to 300 MHz buffered inputs to filters;
- Butterworth 4<sup>th</sup> or 8<sup>th</sup> (Note 1) order switched capacitor LPF from analog input buffer to ADC input;
- Butterworth 5<sup>th</sup> order passive LPF from analog input buffer to ADC input;
- DC to 300 MHz buffer from DAC to Analog Output; DC offset of approximately 1.1 V;
- Butterworth 4<sup>th</sup> or 8<sup>th</sup> (Note 1) order switched capacitor LPF from DAC buffer to analog output buffer;
- Butterworth 5<sup>th</sup> order passive LPF from DAC buffer to analog output buffer;
- Wideband analog output buffer can drive 50 ohm load;
- Analog inputs and output connectors are BNC;
- Powered via host board (3.3 V analog and 3.3 V digital) or 5-7.5 VDC input;
- DC offset reference voltage available as an output;
- Mates with Digilab 10Kx240 or 20Kx240 prototyping boards.

Notes: 1- The 8<sup>th</sup> order function is actually two 4<sup>th</sup> order filters cascaded.

## 3. Glossary

ADC	Analog-to-Digital Converter
BNC	Coaxial connector used for analog signals
DAC	Digital-to-Analog Converter
LPF	Low Pass Filter
MSPS	Million Samples Per Second; ADC conversion rate

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## 4. Board Description

This section gives a detailed hardware description, including option settings, of the HSA. Refer to the HSA schematic for this description.

### 4.1 Power

Separate digital, 3.3VDD, and analog, 3.3VA, power is used on the board. Digital power is nominally 3.3 V at 30 mA. Analog power is nominally 3.3 V at 200 mA. Jacks and option jumpers allow the host board to directly supply both voltages; or, the local voltages can be derived via HSA linear regulators. Input to the linear regulators (J9) must be between 5 and 7.5 volts DC, minimum of 300 mA. Diodes protect against reversed polarity on these inputs, but, no current limiting is included.

The following table shows powering options and connections to HSA jacks and jumpers.

<b>HSA Power Options</b>					
<i>Option</i>	<i>HSA-J16</i>	<i>HSA-J21</i>	<i>HSA-J4</i>	<i>HSA-J5</i>	<i>HSA-J9</i>
Digilab Host	Digilab-P3B	Digilab-P3B	OPEN	OPEN	NC*
Local	NC	NC	CLOSED	CLOSED	5-7.5 VDC

\* NC- No Connect

Pin and signal details are given in Tables 2-4 and Tables 21 and 22, at the end of this manual. It may be necessary to add headers to the appropriate pins of the Digilab host P3B footprint. Two wire cables are provided for connecting to Digilab host power. Pay careful attention to the polarity when using these cables since they are not keyed.

Since all analog devices operate from a single supply voltage, a bias voltage is needed to shift the analog signals above ground to allow peak-to-peak voltage swings. This bias voltage is, nominally, the analog supply voltage divided by three (1.1 V) and is available to the user via J14; see Table 5 for details.

### 4.2 Analog Inputs

Two BNC connectors provide the analog inputs. Each BNC corresponds to an independent input channel. The two channels are designated Analog In-A, J19, and Analog In-B, J20.

#### 4.2.1 Analog In-A

An option jumper allows the BNC connector to be connected either directly to the ADC or through the signal conditioning path, then to the ADC. The signal conditioning circuit topology will support either AC or DC input coupling by changing some of the passive components. The following table summarizes options for Analog In-A. Each option jumper is a three pin header with a two position shorting connector. The table indicates which pins to connect together.

<b>Analog In-A (J19) Options</b>				
<i>Option</i>	<i>HSA-J12</i>	<i>HSA-J1</i>	<i>HSA-J8</i>	<i>HSA-J6</i>
Direct to ADC	2-3	*	*	2-3
4 <sup>th</sup> Order Filter, Local Oscillator	1-2	1-2	1-2	1-2
4 <sup>th</sup> Order Filter, FPGA Clock	1-2	1-2	2-3	1-2
8 <sup>th</sup> Order Filter, Local Oscillator	1-2	2-3	1-2	1-2
8 <sup>th</sup> Order Filter, FPGA Clock	1-2	2-3	2-3	1-2

\* Don't Care

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The user may create a DC path through the filter by replacing C24 with a resistor. Note, care must be taken when replacing C24 with a resistor, as it will change the effect of the VBIAS input to the op-amp. The ADC uses VBIAS as a reference, i.e. the ADC will output digital zero when the ADC input voltage is equal to VBIAS - 0.5 V. Thus, putting a resistor in place of C24 can cause a DC shift away from VBIAS at the output of the op-amp, which drives the ADC input.

One possible DC input configuration would be to replace C24 with a 0 ohm resistor and remove R26. The latter eliminates VBIAS as an input to the op-amp. With this configuration the user must ensure that the input at Analog In-A is referenced to VBIAS (available at J14) in order to get the required ADC input range of VBIAS +/- 0.5 V.

Other DC configurations are possible, including the use of R37 to adjust op-amp gain.

The next section describes the Analog In-A signal conditioning path.

### 4.2.2 Channel A Filter

The following description is for the default, AC coupling path (i.e. C24=10uF). Input impedance at J19 is approximately 50 ohms. The first stage of the signal conditioning path consists of an AC coupled buffer amplifier (U9). The buffer is a high bandwidth, single supply, op-amp. Since the op-amp is a single supply device, the non-inverting input is referenced to a DC voltage, VBIAS, to center the output swing around a bias voltage. VBIAS is approximately the analog supply voltage divided by three. An additional resistor (R37) is included in the layout to provide a means to add gain to the buffer. This optional resistor is normally not included in the assembly. The maximum peak-to-peak (p-p) voltage swing at the output of the buffer should not exceed 1 Vp-p. This stage has a usable bandwidth of about 32 Hz to 300 MHz.

Following the buffer amplifier is a switched capacitor filter (U5). The single IC, an LTC1068-25, is configured as two, fourth order, Butterworth, LPFs. The cutoff frequency of both filters is determined by the input clock frequency. Two options are provided for this clock frequency: 1) an on-board oscillator (nominally 1.0 MHz) can be selected or, 2) an output from the host board can drive the clock input to the LTC1068-25. Cutoff frequency is the input clock divided by 25. Either a single fourth order filter output or, two cascaded fourth order filters, i.e. eighth order output, can be connected to the ADC input. The eighth order function has 6 dB loss at the cutoff frequency, rather than 3 dB, due to the cascaded fourth order filters.

### 4.2.3 Analog In-B

An option jumper allows the BNC connector to be connected either directly to the ADC or through the signal conditioning path, then to the ADC. The signal conditioning circuit topology will support either AC or DC input coupling by changing some of the passive components. The following table summarizes options for Analog In-B. Each option jumper is a three pin header with a two position shorting connector. The table indicates which pins to connect together.

<b>Analog In-B (J20) Options</b>		
<i>Option</i>	<i>HSA-J13</i>	<i>HSA-J2</i>
Direct to ADC	2-3	2-3
Passive Filter	1-2	1-2

The user may create a DC path through the filter by replacing C25 with a resistor. Note, care must be taken when replacing C25 with a resistor, as it will change the effect of the VBIAS input to the op-amp. The ADC uses VBIAS as a reference, i.e. the ADC will output digital zero when the ADC input voltage is equal to VBIAS - 0.5 V. Thus, putting a resistor in place of C25 can cause a DC shift away from VBIAS at the output of the op-amp, which drives the ADC input.

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One possible DC input configuration would be to replace C25 with a 0 ohm resistor and remove R29. The latter eliminates VBIAS as an input to the op-amp. With this configuration the user must ensure that the input at Analog In-B is referenced to VBIAS (available at J14) in order to get the required ADC input range of VBIAS +/- 0.5 V.

Other DC configurations are possible, including the use of R38 to adjust op-amp gain.

The next section describes the Analog In-B signal conditioning path.

### 4.2.4 Channel B Filter

The following description is for the default, AC coupling path (i.e. C25=10uF). Input impedance at J20 is approximately 50 ohms. The first stage of the signal conditioning path consists of an AC coupled buffer amplifier (U10). The buffer is a high bandwidth, single supply, op-amp. Since the op-amp is a single supply device, the non-inverting input is referenced to a DC voltage, VBIAS, to center the output swing around a bias voltage. VBIAS is approximately the analog supply voltage divided by three. An additional resistor (R38) is included in the layout to provide a means to add gain to the buffer. This optional resistor is normally not included in the assembly. The maximum peak-to-peak (p-p) voltage swing at the output of the buffer should not exceed 1 Vp-p. This stage has a usable bandwidth of about 32 Hz to 300 MHz.

Following the buffer amplifier is a Passive, fifth order, Butterworth, LPF. The two inductors (L1 and L2) are surface mount 1210 packages. The three capacitors (C8, C9, and C14) are 1206 packages. The load resistor (R7) is an 0805 package. This filter is referenced to the same bias voltage as the buffer amplifier, rather than ground, to minimize the DC current flowing in the inductors. With the installed components the cutoff frequency is 2 MHz. The user may adjust this cutoff frequency by changing the inductor and capacitor values. See section 5 for determining component values.

### 4.2.5 Analog-to-Digital Converter

A two channel, 8-bit converter, the AD9288 (U4, 40 MSPS), is provided. Each channel can be independently configured to accept either the direct or filtered input from the corresponding analog input. The inverting input of each ADC channel is referenced to the same bias voltage, VBIAS, as the buffer amplifiers. This provides a DC offset that allows the input signal to swing 0.5V above or below the bias voltage.

Either offset binary or twos-complement output can be selected via a signal driven by the host board (DFS). The output format of both channels is selected by this one signal.

<b>ADC Output Format Options</b>	
<i>DFS</i>	<i>Output</i>
0	Offset binary
1	Two's complement

Jumpers allow the setting of the User Select Options (S1 & S2). Each option jumper is a three pin header with a two position shorting connector. The table indicates which pins to connect together.

<b>ADC User Options</b>			
<i>S2, S1</i>	<i>HSA-J3</i>	<i>HSA-J7</i>	<i>User Option</i>
0,0	2-3	2-3	Standby both channels
0,1	2-3	1-2	Normal operation
1,0	1-2	2-3	Standby channel B only
1,1	1-2	1-2	Data align enabled

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See the AD9288 Data Sheet for a description of ADC user options.

The conversion clock input for each channel comes from two signals driven by the host board: ADC\_ENCA for channel A, and ADC\_ENCB for channel B. A new sample is generated on each rising edge of ADC\_ENCA/B. Due to the internal logic of the AD9288, there is a four clock cycle delay from input to output.

### 4.3 Analog Output

The Analog Output BNC connector (J18) can be connected either directly to the DAC buffer amplifier (U13), or through the analog output signal conditioning path. The following table shows all the analog output options. Each option jumper is a three pin header with a two position shorting connector. The table indicates which pins to connect together.

Analog Out (J18) Options					
Option	HSA-J11	HSA-J22	HSA-J15	HSA-J17	HSA-J10
Direct to DAC Buffer	2-3	OPEN	*	*	*
4 <sup>th</sup> Order Filter, Local Oscillator	1-2	1-2	1-2	1-2	1-2
4 <sup>th</sup> Order Filter, FPGA Clock	1-2	1-2	1-2	1-2	2-3
8 <sup>th</sup> Order Filter, Local Oscillator	1-2	1-2	1-2	2-3	1-2
8 <sup>th</sup> Order Filter, FPGA Clock	1-2	1-2	1-2	2-3	2-3
Passive Filter	1-2	2-3	2-3	*	*

\* Don't Care

#### 4.3.1 Output Filters

The signal conditioning path has two options. The first option is a switched capacitor filter (U12). The single IC, an LTC1068-25, is configured as two, fourth order, Butterworth, LPFs. The cutoff frequency of both filters is determined by the input clock frequency. Two options are provided for this clock frequency: 1) an on-board oscillator (nominally 1.0 MHz) can be selected or, 2) an output from the host board can drive the clock input to the LTC1068-25. Cutoff frequency is the input clock divided by 25. Either a single fourth order filter output or, two cascaded fourth order filters, i.e. eighth order output, can be connected to the analog output buffer. The eighth order function has 6 dB loss at the cutoff frequency, rather than 3 dB, due to the cascaded fourth order filters.

The second option for the signal conditioning path is a Passive, fifth order, Butterworth LPF. The two inductors (L3 and L4) are surface mount 1210 packages. The three capacitors (C26, C27, and C35) are 1206 packages. The load resistor (R43) is an 0805 package. This filter is referenced to the same bias voltage as the buffer amplifier, VBIAS, rather than ground, to minimize the DC current flowing in the inductors. With the installed components the cutoff frequency is 2 MHz. The user may adjust this cutoff frequency by changing the inductor and capacitor values. See section 5 for determining component values.

A buffer amplifier (U8) drives the output BNC connector. The bandwidth of this buffer, assuming a 50 ohm load, is 318 Hz to 300 MHz. Replacing C23 with a resistor will allow the buffer amplifier to drive a DC output.

#### 4.3.2 DAC Buffer

A single-supply op-amp (U13) converts the differential outputs of the DAC to a single-ended signal. This op-amp is a high bandwidth device. It also provides a buffer stage capable of driving 50 ohm loads. Since

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the op-amp is a single supply device, the non-inverting input is referenced to a DC voltage to center the output swing around a bias voltage. This bias voltage, VBIAS, is approximately the analog supply voltage divided by three (1.1 V).

### 4.3.3 Digital-to-Analog Converter

A single-channel, 8-bit converter, the MAX5190 (U11), is provided. The differential outputs swing from 0 to 400 mV. The clock input is driven by a host board signal, DAC\_CLK. The maximum frequency is 40 MHz. See the MAX5190 Data Sheet for details about DAC operation.

### 4.4 Connectors

A 50 pin connector (JP1) provides the interface to either the Digilab 10Kx240 or 20Kx240 FPGA prototyping board. The HSA connects to P3A of either board. See Table 1 for pinout.

HSA power can be provided by the 10Kx240/20Kx240 VCCIO and VCC\_AUX linear regulators. A two pin header (J16) is used to connect 3.3VDD to VCCIO on connector P3B of the Digilab board. Similarly, another two pin header (J21) is used to connect 3.3VA to VCC\_AUX on P3B of the Digilab board. Note, the Digilab board must be configured to source 3.3 volts for VCCIO and VCC\_AUX. Also, mating 2 pin headers will need to be soldered into P3B at the appropriate pin locations. Cables are provided to make these power connections. See Tables 2 and 3.

Pins 2 and 4 of P3A are no-connects on the Digilab 10Kx240 and 20Kx240. The HSA connects pins 2 and 4 of JP1 to 3.3VA and 3.3VDD respectively, as another means of providing host power to the HSA.

A two position terminal connector (J9) is provided for an optional DC voltage input. This is only used if power is not supplied by the Digilab board. See Table 4.

A two pin header (J14) provides access to the HSA VBIAS voltage. See Table 5.

Standard BNC connectors, two for analog inputs (J19 and J20) and one for analog output (J18), are provided. See Tables 6 through 8.

Multiple 3 pin option jumpers are located on the board to allow various configuration settings. See Tables 9 through 23.

A prototyping area (PA1), which consists of plated holes with access to power and ground, is provided on the PWB.

## 5. Passive Filter Component Calculations

The passive filter is a standard 5<sup>th</sup> order Butterworth LC ladder. Component values can be calculated for a given 3dB cutoff frequency,  $\omega_0$ , using the following formulae.  $R_0$  is the termination and source impedance;  $C_1 = C_5$  are the outside capacitors;  $C_3$  is the middle capacitor;  $L_2 = L_4$  are the inductors (these reference designators are only for the formulae and do not correspond to schematic components).

$$C_1 = C_5 = ( 0.618 / R_0\omega_0 )$$

$$C_3 = ( 2.0 / R_0\omega_0 )$$

$$L_2 = L_4 = ( 1.618 R_0 / \omega_0 )$$

You must choose available component values as close as possible to the calculated values.

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## 6. Tables

Table 1- Host Connector, JP1			
<i>Signal Name</i>	<i>Pin #</i>	<i>Pin #</i>	<i>Signal Name</i>
GND	1	2	3.3VA
NC*	3	4	3.3VDD
NC	5	6	TP2**
DFS	7	8	TP1
FILTER_CLK2	9	10	DAC_CLK
DACD0	11	12	FILTER_CLK1
DACD2	13	14	NC
DACD4	15	16	DACD1
GND	17	18	NC
DACD6	19	20	DACD3
ADCD1A	21	22	DACD5
ADCD3A	23	24	DACD7
ADCD5A	25	26	ADCD0A
NC	27	28	NC
ADCD7A	29	30	ADCD2A
NC	31	32	ADCD4A
GND	33	34	NC
NC	35	36	ADCD6A
ADC_ENCA	37	38	ADC_ENCB
ADCD0B	39	40	ADCD1B
ADCD2B	41	42	ADCD3B
ADCD4B	43	44	ADCD5B
ADCD6B	45	46	ADCD7B
NC	47	48	ADCD4B @
GND	49	50	NC

\* NC- no connect

\*\* TP- test point

@ Necessary for 20Kx240 host

Table 2- 3.3VDD Input, J16		
<i>HSA, J16 Pin #</i>	<i>Digilab P3B, Pin #</i>	<i>Signal Name</i>
1	60	VCCIO
2	59	GND

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Table 3- 3.3VA Input, J21		
<i>HSA, J20 Pin #</i>	<i>Digilab P3B, Pin #</i>	<i>Signal Name</i>
1	68	VCC_AUX
2	67	GND

Table 4- DC Input, J9	
<i>Header Pin #</i>	<i>Signal</i>
1	DC Positive
2	GND

Table 5- Reference Output, J14	
<i>Header Pin #</i>	<i>Signal</i>
1	Ref. Positive
2	GND

Table 6- Analog Output, J18	
<i>BNC Pin #</i>	<i>Signal</i>
1	Analog Out
2	GND

Table 7- Analog Input, J19	
<i>BNC Pin #</i>	<i>Signal</i>
1	Analog In-A
2	GND

Table 8- Analog Input, J20	
<i>BNC Pin #</i>	<i>Signal</i>
1	Analog In-B
2	GND

Table 9- Option Jumper J11	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	DAC filter to Analog Out
2-3	DAC buffer to Analog Out

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Table 10- Option Jumper J12	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Analog In-A to switched cap filter
2-3	Analog In-A direct to ADC channel A

Table 11- Option Jumper J13	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Analog In-B to passive filter
2-3	Analog In-B direct to ADC channel B

Table 12- Option Jumper J1	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Sw. cap 4 <sup>th</sup> order output to ADC channel A
2-3	Sw. cap 8 <sup>th</sup> order output to ADC channel A

Table 13- Option Jumper J8	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Local osc. input to ADC sw. cap filter
2-3	Host clock input to ADC sw. cap filter

Table 14- Option Jumper J6	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Sw. cap filter input to ADC channel A
2-3	Analog In-A input to ADC channel A

Table 15- Option Jumper J7	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	ADC pin S1 high
2-3	ADC pin S1 low

Table 16- Option Jumper J3	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	ADC pin S2 high
2-3	ADC pin S2 low

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Table 17- Option Jumper J2	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Passive filter input to ADC channel B
2-3	Analog In-B input to ADC channel B

Table 18- Option Jumper J10	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Local osc. input to DAC sw. cap filter
2-3	Host clock input to DAC sw. cap filter

Table 19- Option Jumper J17	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	DAC Sw. cap 4 <sup>th</sup> order output to J15
2-3	DAC Sw. cap 8 <sup>th</sup> order output to J15

Table 20- Option Jumper J15	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	DAC Sw. cap output to analog output buffer
2-3	DAC Passive filter output to analog output buffer

Table 21- Option Jumper J4	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Local regulator to 3.3VDD
OPEN	Host VCCIO to 3.3VDD

Table 22- Option Jumper J5	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	Local regulator to 3.3VA
OPEN	Host VCC_AUX to 3.3VA

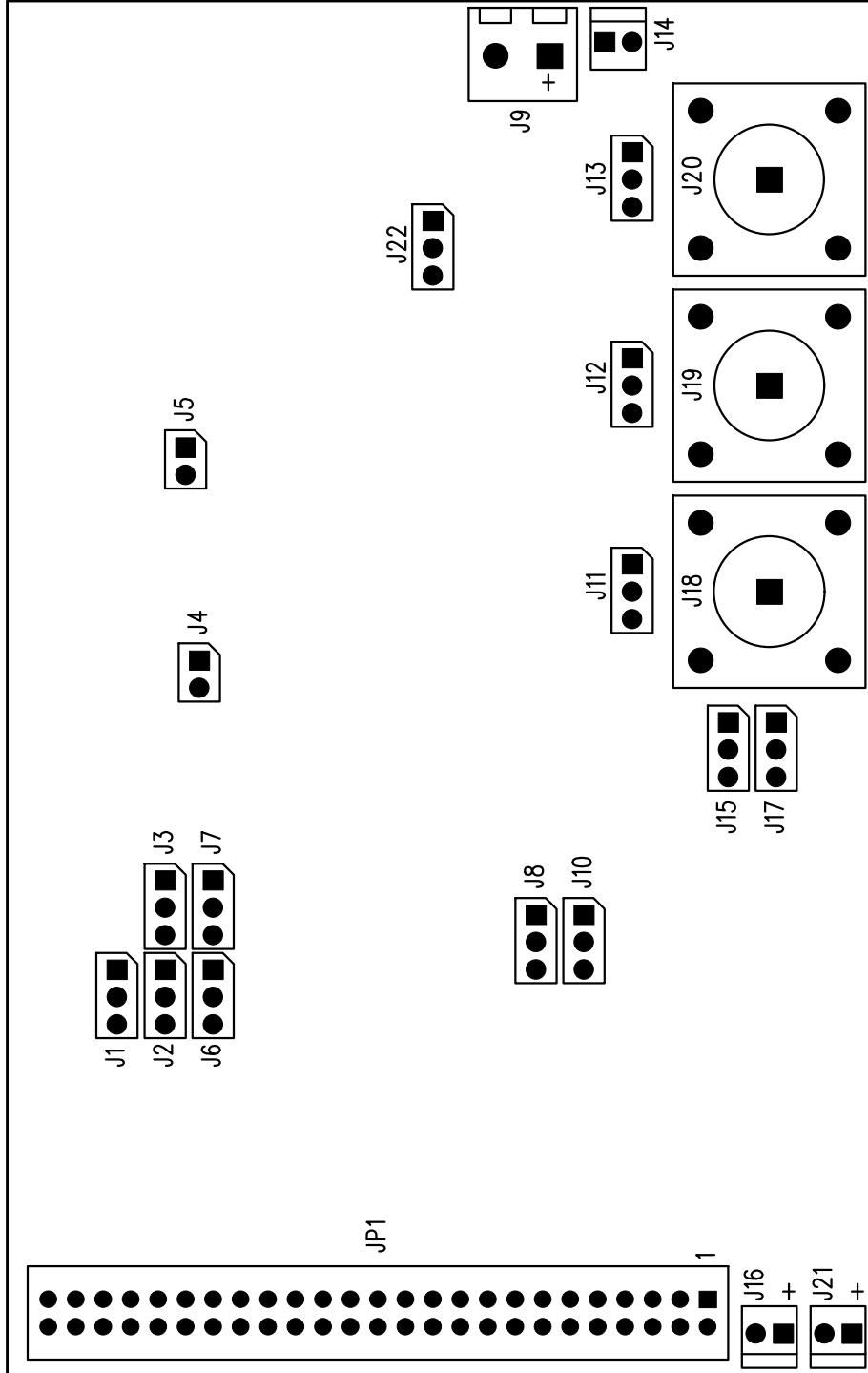
Table 23- Option Jumper J22	
<i>Jumper Pins</i>	<i>Option Selected</i>
1-2	DAC Buffer to Switched Capacitor filter
2-3	DAC Buffer to Passive filter
OPEN	DAC Buffer to J11 only

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## 7. Attachments

A drawing showing jumper locations is attached.

The schematic diagram is attached.



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