

General Description

The DIGILAB Memory module is a universal and flexible memory module. It can be used with El Camino and Altera prototyping boards or for embedded Cyclone based NIOS processor systems.

The module supports up to 512k x 36 synchronous SRAM as well as 2M x 16 or 4M x 8 FLASH memory, connected to a common address and data bus. It comes in a standard 144-pin SODIMM form factor and can be used with any El Camino or Altera prototyping board that offers one or more 144-pin SODIMM sockets.

The memory module offers all storage requirements, necessary for Cyclone based processor systems. There is an Altera EPCS4 serial configuration device that can be used for Cyclone device configuration. A NIOS processor can use FLASH and synchronous RAM for data and program storage.

Features

Preliminary Information

- 512k x 36 synchronous SRAM memory
- 2M x 16 or 4M x 8 FLASH memory
 - FLASH supports Byte mode
 - DQ15/A-1 pin can be disconnected from DQ bus
- All control signals available at connector for flexible use
- FLASH boot sector write protect supported with solder bridge
- Standard 144-pin SODIMM form factor
 - 31.8mm height
- Can be used on any prototyping board with 144-pin SODIMM connector e.g. from
 - El Camino
 - Altera
- Supports Altera serial Flash EPROM
 - Cyclone device configuration
 - Module identification
 - Additional Memory accessible to NIOS processors

Preface

Environmental Requirements

The memory module must be stored between -40°C and 100°C. The recommended operating temperature is between 0°C and 55°C.

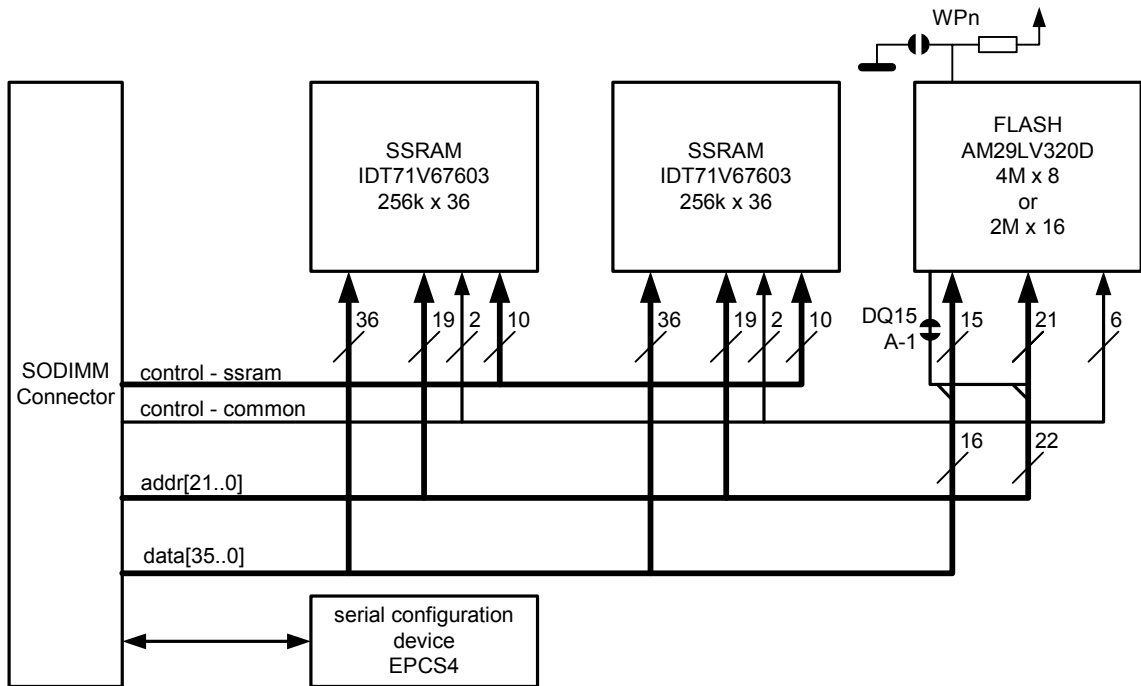


The module can be damaged without proper anti-static handling. Therefore, you should take anti-static precautions before handling the board.

Functional Description

This section describes the elements of the DIGILAB Memory module. Figure 1 shows a block diagram of the module.

Figure 1: DIGILAB Memory Module Block Diagram



SSRAM Memory

The DIGILAB Memory module has two synchronous 256k x 36 IDT SRAM devices. Address line A20 selects between the two chips forming a 512k x 36 memory space. All major control signals can be accessed through the SODIMM connector.

The SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle. The burst mode

feature offers the highest level of performance to the system designer, as the SRAMs can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected (ADV=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the LBO input pin.

A datasheet for the SSRAM devices can be found at:
http://www.idt.com/docs/71V67603_DS_34987.pdf

Refer to the schematic at the end of this data sheet for detailed pin out information.

FLASH Memory

The DIGILAB Memory module is equipped with a 32 megabit, 3.3 volt flash memory device, organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. Word mode data appears on DQ0–DQ15; byte mode data appears on DQ0–DQ7. The device is designed to be programmed in-system with the standard 3.3 volt VCC supply.

The device offers complete compatibility with the JEDEC single-power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors. This function is one of two provided by the WP#/ACC pin. If the WP#/ACC pin is connected to GND by closing the soldering bridge BR2, the device disables program and erase functions in the two “outermost” 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using other methods. The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device. The DIGILAB Memory module uses a bottom-boot-configured device.

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic ‘1’, the device is in word configuration, DQ0–DQ15 are active and controlled by

CE# and OE#. If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

The DQ15/A-1 pin is connected to both A0 and DQ15 pin of the SODIMM connector. Soldering bridge BR1 is closed by default and connects DQ15/A-1 to DQ15. When using the flash chip in byte mode either make sure that A0 (connected also to DQ15) is not driven while data is read from the SSRAM or permanently open BR1 e.g. with a scalpel.



By default SODIMM signal A0 connects to DQ15 of the data bus. Do not drive A0 while SSRAM devices are selected for reading and soldering bridge BR1 is still closed.

A datasheet for the Flash device can be found at:
http://www.amd.com/us-en/assets/content_type/white_papers_and_tech_docs/23579c1.pdf

Serial Configuration Device

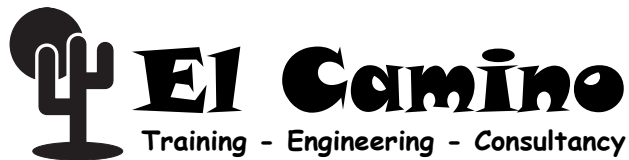
The DIGILAB Memory module features an Altera 4-Mbit flash memory devices that can serially configure Cyclone FPGAs.

With SRAM-based devices such as Cyclone FPGAs, configuration data must be reloaded each time the system initializes, or when a new configuration is needed. Serial configuration devices are flash memory devices with a serial interface that can store configuration data for a Cyclone device and reload the data to the device upon power-up or re-configuration.

A designer can access the unused memory locations of the serial configuration device through the Nios processor and SOPC Builder to store/retrieve data or configuration files. SOPC Builder is an Altera tool for creating bus-based (especially microprocessor-based) systems in Altera devices. SOPC Builder assembles library components like processors and memories into custom microprocessor systems. SOPC Builder includes an interface core specifically for the serial configuration device. Using this core, a designer can create a system with a Nios embedded processor that allows software access to any memory location within the serial configuration device.

A datasheet for the Altera EPCS4 serial configuration Device can be found at:
<http://www.altera.com>

Notes:



El Camino GmbH
Landshuter Str. 1
D-84048 Mainburg
Germany
Telephone +49-8751-8787-0
Telefax +49-8751-842876
E-mail: info@elca.de
<http://www.elca.de>

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