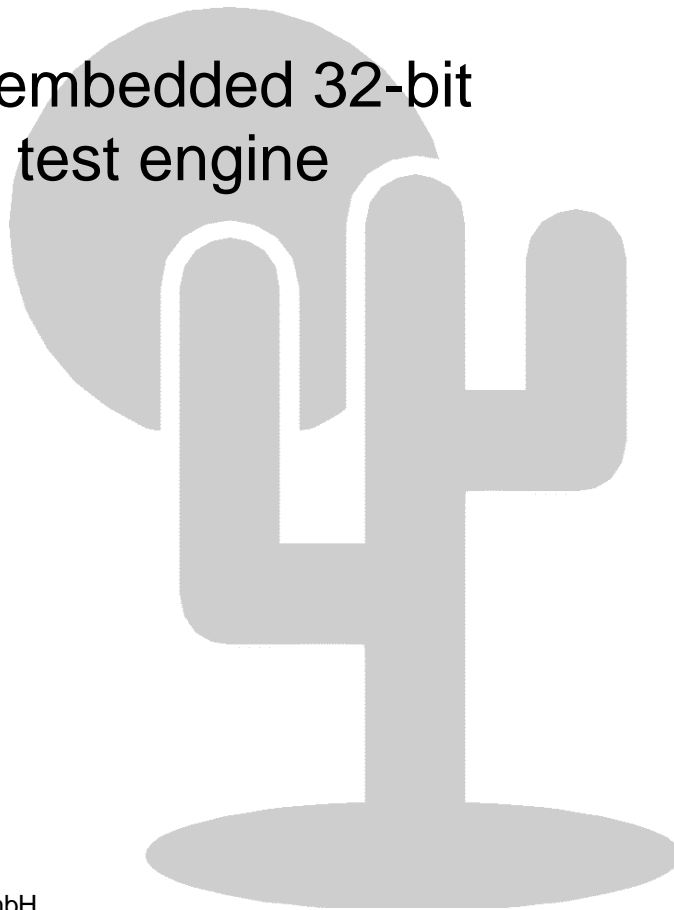


DIGILAB megAPEX MANUAL

APEX™ 20K High-End Prototyping
System

With embedded 32-bit
RISC test engine



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Digilab megAPEX – Preface

General Description

The DIGILAB megAPEX is a high-end modular prototyping system, based on Altera's APEX 20KE/C device families. The speed and density of the megAPEX system supports system integration tests as well as near real time HW/SW co-verification.

DIGILAB megAPEX Features:

- Modular and expandable prototyping system
- Supports up to six Logic-Modules (9 million gates/15 million systems gates total)
- 200+ MHz system operation in single or multi module set-ups

- Logic-Module
 - Any APEX20KE device in BGA652 from EP20K400EBC652 up to the EP20K1500EBC652-1X
 - Comes with on-chip, 32-bit RISC test engine for C/C++-based test pattern generation, pattern checking and on-chip reference data computation
 - Interface to 270 megAPEX user I/Os signals
 - feed in test pattern (i.e. with test pattern generator)
 - log output signals (i.e. with logic analyzer)
 - 1M x 32 FLASH EPROM
 - 1M x 32 fast SRAM
 - Up to six Logic-Modules can be cascaded
 - PLL support for advanced clock generation and clock distribution
 - LVCMOS and LVDS clocking options
 - Two Clock drivers supporting up to six logic-modules each
 - Configuration management
 - JTAG download cable interface
 - Passive Serial Mode download cable interface
 - EPC16 on-board configuration device
 - Push buttons and user LEDs
 - Power management

- Termination-Module
 - Access to additional I/Os
 - Optional termination of GTL+ Bus

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Altera, Quartus, APEX 20K, NIOS, ByteBlaster

We reserve the right to make changes without notice on the boards or specifications described in this document.

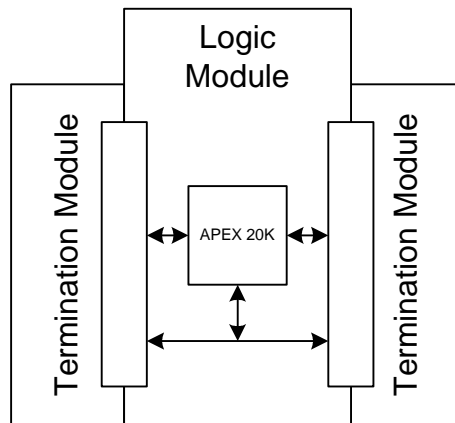
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General Description

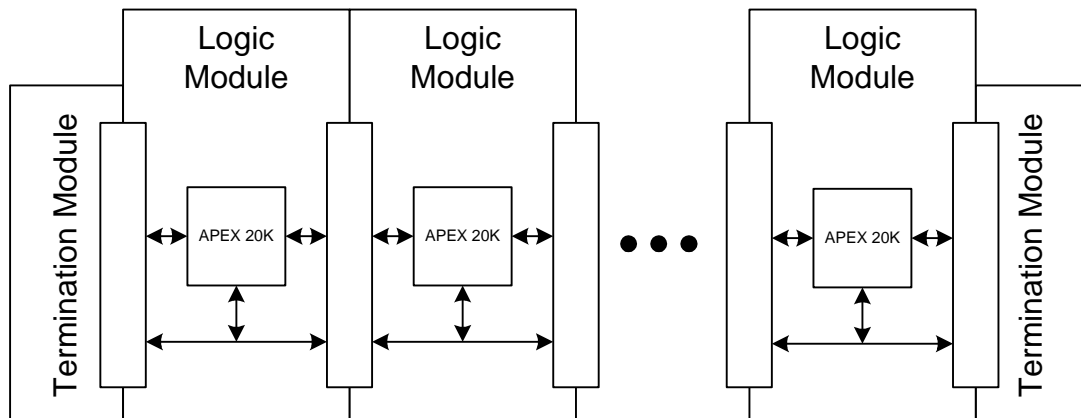
System Block Diagram

The DIGILAB megAPEX is a modular, high-end prototyping system. Up to six logic modules can be cascaded and terminated on both ends with termination boards. The system provides a high number of inter-board connections as well as a high speed common GTL+ bus. The board supports any Altera APEX 20K400, 20K600, 20K1000 or 20K1500 device in Aluminium (E) or Copper (C) technology and a 652 pin BGA package.

A single module set-up supports one APEX 20K device with up to 1.5 million gates (3 million system gates) or more than 52,000 FlipFlops.



In a multi module setup up to six logic modules can be cascaded with more than 300,000 FlipFlops available for prototyping.



Prototyping Environment

Test Concept

The DIGILAB megAPEX supports a new and unique prototyping approach. It comes with a 32-bit RISC soft core processor, optionally instantiated in a VHDL or Verilog test wrapper. The RISC processors can be connected to the device under test within the wrapper through a flexible number of on-chip input and output ports.

This new concept allows to implement on-chip C/C++ based test pattern generation, pattern checking and on-chip reference models.

The processor uses SRAM and FLASH memory, available on each megAPEX board. It can be controlled through the RS232 interface and a basic monitor program, running from on-chip ESB (APEX 20K embedded system blocks) memory. The processor runs at up to 50 MHz, approximately equivalent to 44 MIPS. By using the monitor program together with some simple commands it is possible to statically set and test hundreds of on-chip I/Os. Additionally the monitor program may be used to download complex C/C++ programs to either SRAM or FLASH (4 Mbytes each) and start these programs. The transfer of debug information or menu driven control over a test can be accomplished through the RS232 interface and a standard terminal program running on a PC.

The 32-bit RISC test engine is based on Altera's soft core NIOS processor. In order to develop C/C++ base test software the Altera NIOS Software Development Kit (NIOS-GNUPRO) is required which is available at US-\$ 495,- directly from Altera. On the enclosed disk there's a "megAPEX_sdk" directory which contains all the libraries and include files for custom software projects. Alternatively it is also possible to purchase the complete EXCALIBUR-NIOS Kit from Altera at US-\$ 995,- which gives access to both the development environment and the parameterizeable NIOS 32-bit RISC core. This allows to customize the RISC test engine and add any number of UARTs, parallel I/Os, Timers, I²C, SPI and more peripherals interfacing to the device under test or even add more processor cores.

Please see the Altera Excalibur NIOS information, available from the Altera website for more details. Especially there are:

- Nios Embedded Processor Software Development Reference Manual
- Nios Embedded Processor Programmer's Reference Manual

VHDL/Verilog Wrapper with optional 32-bit test engine

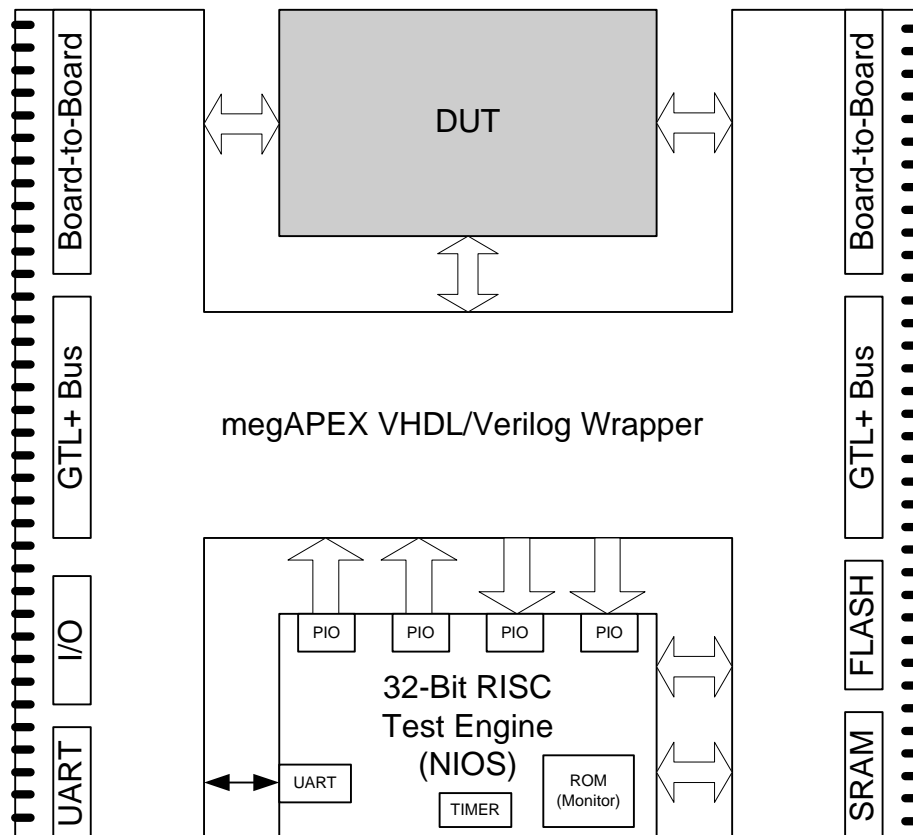
On the enclosed disk there are VHDL and Verilog wrapper as well as a Quartus TCL script for making pin assignments.

The wrapper has all the available megAPEX I/O ports instantiated and well documented. It can be used to easily instantiate a DUT component and connect all DUT I/Os to the available resources on the megAPEX board. Within the wrapper board-to-board and GTL+ bus signals are defined as inout. It is up to the user to connect either inputs, outputs or bi-directional signals and make sure that there are no contentions when multiple modules are used.

Additionally the wrapper instantiates an optional 32-bit RISC test engine. This processor is already connected to the on-board SRAM and FLASH memory as well as to the on-board UART. The test engine comes with two 32-bit output ports and two 32-bit input ports that are available on-chip or can also be connected to off-chip resources through the VHDL/Verilog wrapper. When not required the processor component can be removed and the UART, SRAM and FLASH be used for custom functions.

Please refer to the comments within the wrapper for further details on the available signals and their names.

The included TCL script sets all the pin-assignments for APEX device on the board so that the user only needs to decide how to connect the DUT to the available signals.



32-bit RISC test engine

To connect to the on-chip processor a design including the test-engine needs to be downloaded first. A standard terminal program can be used to communicate with the GERMS Monitor program of the test engine. The UART of the processor has been built to work at 115k Baud with a 24 MHz system clock. When using a different system clock frequency for the processor it is necessary to re-parameterize and re-build the NIOS core.

Baud Rate	Parity	Data Bits	Stop Bits	Flow Control	Necessary System Clock
115000	N	8	2	none	24 MHz

Monitor Commands

- **Go**
Execute a CALL instruction to the specified address.
Syntax: G<address>
<address> is any number of hexadecimal digits
Example: G400100
Nios runs until done
- **Erase**
Erase Flash Memory
If the address is within the range of the "flash" ROM, the sector containing that address will be erased
Syntax: E<address>
<address> is any number of hexadecimal digits
Example: E1000000
- **Relocate**
Relocate next download to this address
Next S-record or I-Hex record will be stored starting at this address
Syntax: R<address>
<address> is any number of hexadecimal digits
Example: R1000000
- **Display/Write Memory**
Display a range of memory
Write successive 16-bit words to memory
Fill a range of memory with a 16-bit word
Syntax: M<address> - <address> M400000-400100
M<address> M400000
M<address> : <value> <value> <value> M400000:feff 43 6f5
M<address> - <address> : <value> M400000-400100:dead
- **S-Record**
Accept an S-record
Syntax: S<S-record data>
Example: S<218400000 . . . >
Usage: Terminal programs (e.g. Hyperterm) can download an srec file by "transferring" the file to the COM port

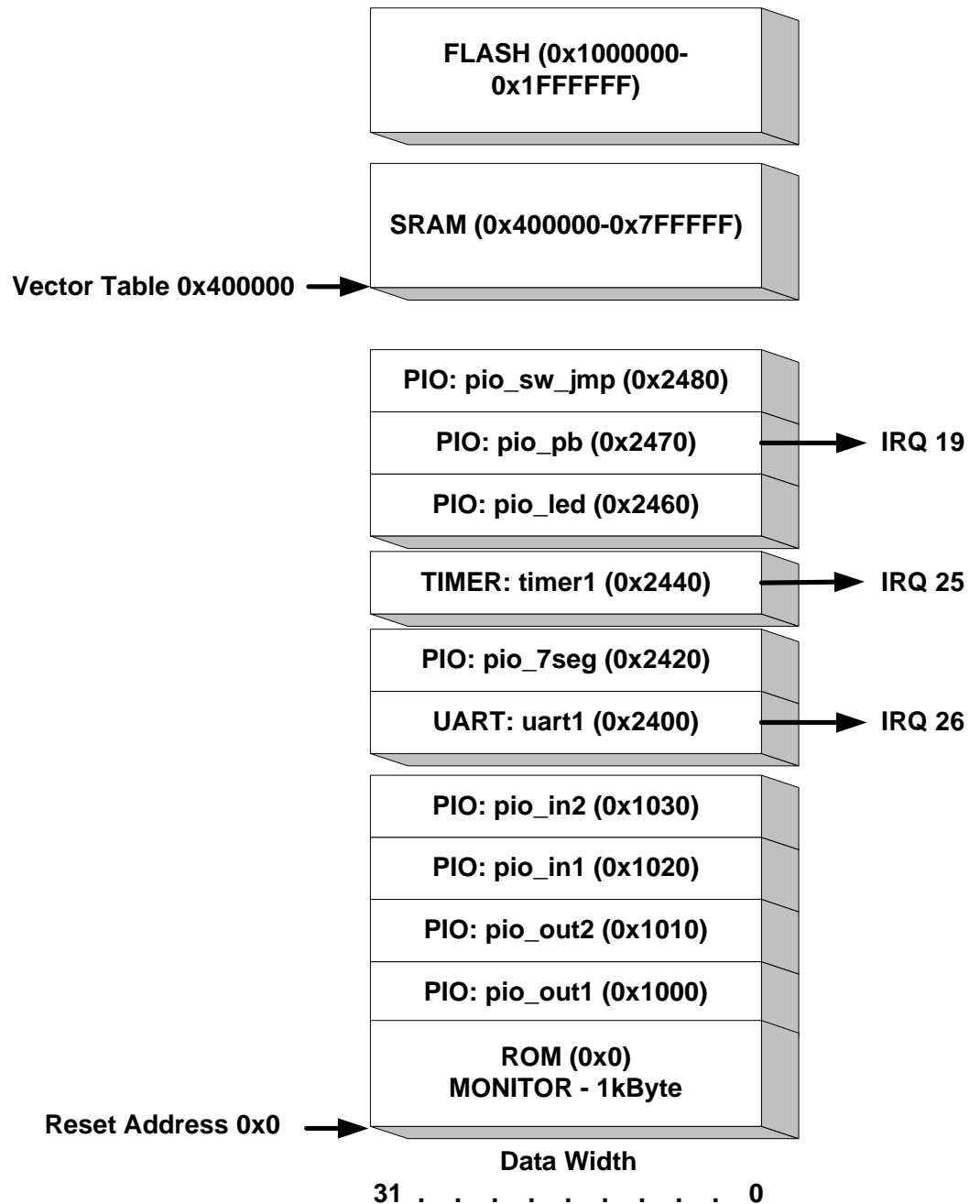
- I-Hex record**
 Syntax: :<l-Hex record data>
 Example: :80000004
 Usage: Terminal programs (e.g. Hyperterm) can download an I-Hex file by
 “transferring” the file to the COM port

- Display the next 16 bytes of memory**
 Syntax: <CR>
 Usage: r0
 #0000: 4A4C 3189 9808 0409 8868 3000 4950 9820
 +
 #0010: 3604 35E5 3466 3413 3414 3415 8917 3000
 +
 #0020: 9806 7F29 891F 3000 890B 35A8 8909 3548

 m0
 #0000: 4A4C 3189 9808 0409 8868 3000 4950 9820
 +
 #0010: 3604 35E5 3466 3413 3414 3415 8917 3000
 +
 #0020: 9806 7F29 891F 3000 890B 35A8 8909 3548

Address Map

The following diagram shows the address map of the included, pre-compiled processor. Datasheets on all the peripherals can be found on the Altera web site.



Hardware Block Diagrams

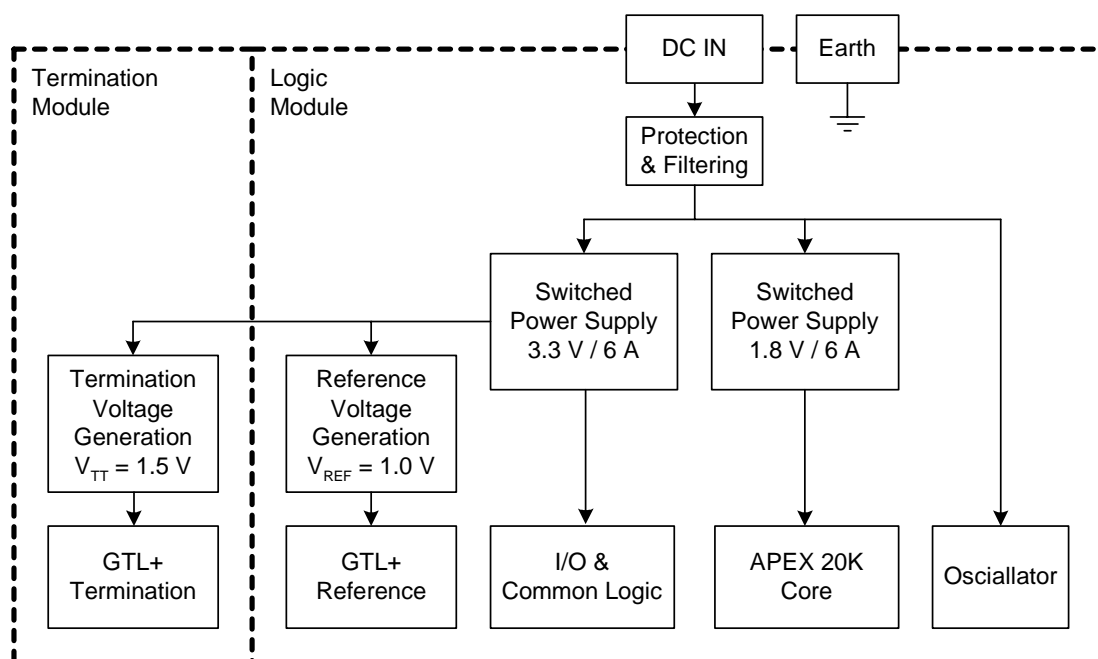
Power Management

Each DIGILAB megAPEX logic module has its own power supply and power management. There's one common input that supplies the complete board as well as optional termination modules on each side of the board.

The fuse F1 limits the maximum total input current to 10A and provides in conjunction with D5 a protection from mixed-up input polarity. A blown F1 has to be de-soldered and replaced with an equivalent 10A fuse.

Power Specification:

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage, Absolute Maximum	$V_{I_{max}}$	-	-	7.0	V_{DC}
Operating Input Voltage	V_I	4.5	5.0	5.5	V_{DC}
Maximum Input Current	$I_{I_{max}}$	-	-	10	A
Available current to APEX V_{CCINT}	I_{VCCINT}	-	-	6	A

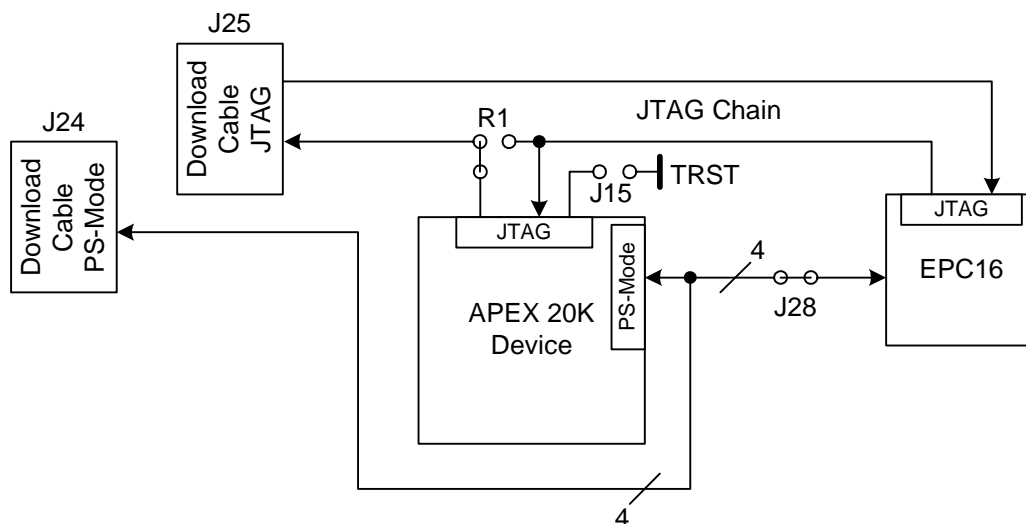


Please refer to the schematics for further details on the power supply circuitry.

Configuration

There are various different ways to configure the DIGILAB megAPEX modules. Each module needs to be configured individually. There's a JTAG chain on each module starting at J25 going through the EPC 16 configuration device and the APEX 20K device. By changing R1 from 1-2 to 1-3 and setting J15 the APEX device can be removed from the JTAG chain and held in a JTAG reset state (some EP20K1500 devices have faulty JTAG logic).

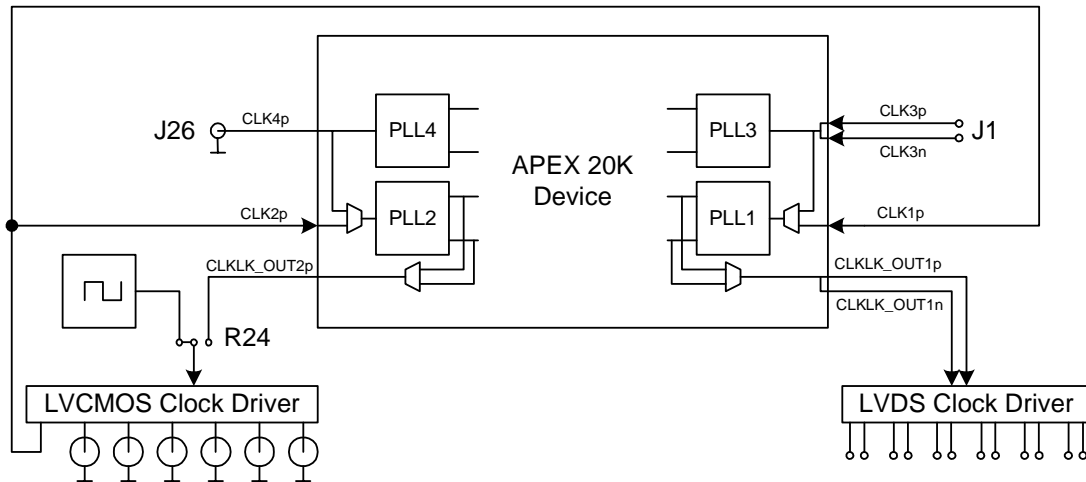
1. APEX configuration through JTAG Port – Volatile
J25 can be used to connect an Altera download cable to the DIGILAB megAPEX module and configure the APEX device in JTAG mode. There are only two devices in the JTAG chain, the EPC16 configuration device followed by the APEX device (some EP20K1500 device don't support JTAG configuration because of faulty JTAG logic).
2. APEX configuration through Passive Serial Port – Volatile
J24 can be used to connect an Altera download cable and configure the APEX device in Passive Serial Mode. When using this mode it is important to disconnect the EPC 16 device from the APEX passive serial configuration interface. This can be done by removing all J28 jumpers. Not doing so will cause contentions and possible damage the EPC 16 device.
3. EPC16 Programming through JTAG Port - Non-Volatile
J25 can also be used to connect an Altera download cable and program the EPC 16 device through it's JTAG interface. After programming the EPC 16, MAX+plus II and Quartus support commands to initiate configuration of the APEX device with the new EPC 16 content. Upon power up the APEX device will automatically try to configure from the EPC 16. Setting J29 disables automatic configuration from the EPC 16.



Please refer to the schematics for further details on the configuration circuitry.

Clock Distribution

The DIGILAB megAPEX supports various, flexible clocking schemes. One board can drive up to six modules with both LVCMOS and LVDS clocks.



There's an on board 5V oscillator that can drive the LVCMOS clock driver (default setting of R24). 5V was chosen because of the better availability of these devices. The oscillator can be easily exchanged with other devices with different frequencies. Since APEX 20KE devices are not 5V tolerant, one output of the LVCMOS clock driver is connected to CLK1 and CLK2 inputs of the APEX device and drives PLL1 and PLL2 respectively.

The LVCMOS clock driver outputs of a single module can be used to synchronously drive up to six cascaded megAPEX modules (J26 input / CLK4). CLK4 has an optional termination network (R51/CA101). In this mode the oscillator frequency is directly distributed to all boards. PLL4 and PLL2 can be used to generate up to 4 derived clocks inside the APEX device. Alternatively PLL1 can be used to modify the oscillator frequency and distribute a high speed LVDS clock to up to six modules.

Both PLL feedback inputs are routed to test points and might be used for external feedbacks. Furthermore the lock outputs are available at test points (TP101, 102, 103, 104) and also routed back to I/O pins of the APEX device for internal usage. When using external PLL feedbacks the PLLs must not be enabled before configuration is complete, which can be accomplished by using the external connection between the optional INITDONE and CLKLK_ENA pins. There's a test point (TP111) at this connection for further flexibility.

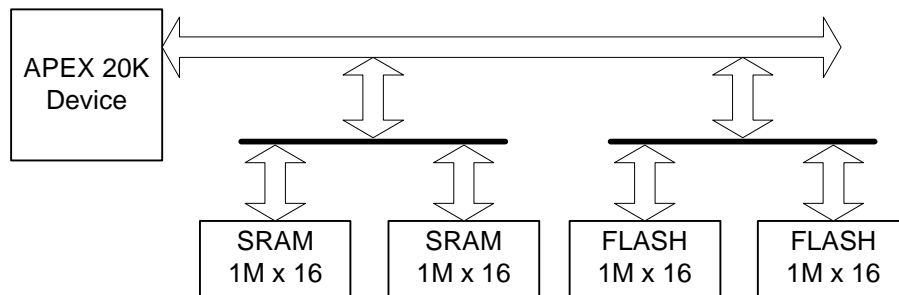
There are many more possible clocking schemes and combinations which might be chosen based on application or prototyping requirements.

Please refer to the schematics for further details on clocking options.

RAM/FLASH

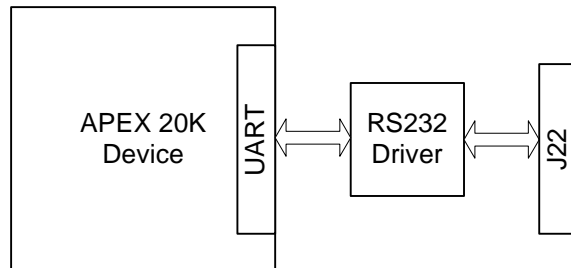
The DIGILAB megAPEX has a total of 4 MBytes of fast SRAM and 4 MB of FLASH memory. There's a shared data- and address- bus for both SRAM and FLASH. All data, address and control signals are dedicated to the memory and can't be used for other purposes. Furthermore these signals are not available at test points or connectors.

The memory banks can be used e.g. to implement one or more NIOS processor cores inside the APEX device. These 32-bit RISC processors can be used for on chip test pattern generation or pattern checking.



Serial Interface – RS232

The DIGILAB megAPEX supports a RS232 interface with optional RTS/CTS. To use this interface a UART needs to be implemented inside the APEX device. It can be utilized to communicate to an on chip processor like the Altera NIOS or to communicate to other custom logic.



Buttons, Switches and LEDs

The DIGILAB megAPEX has the following basic I/O features for debug purposes:

1. Global reset push button (SW100)
This push button drives the optional DEV_CLRn input. When the APEX 20K option "Enable device wide reset (DEV_CLRn)" is turned on, this push button can be used to clear all registers inside the APEX device independent of clear usage in the design being implemented.
When the APEX option is not selected the input connected to this button behaves like a general purpose I/O and can be used to drive clear/preset logic implemented in the design.
2. Three debounced custom push buttons (SW101, 102, 103)
These three buttons are debounced and connected to general purpose I/Os. They can be used for any custom input functions. When pushed these buttons drive logic low.
3. Four DIP switches
There are four on board DIP switches connected to general purpose I/Os for custom usage.
4. Status LED - NSTATUS (D1)
Indicates a configuration error when on.
5. Status LED - CONFDONE (D2)
Indicates configuration was successful when on.
6. Two LEDs for custom use (D3 - D4)
D3 and D4 are LEDs connected to general purpose I/Os. These LEDs can be used for custom functions. When driven low these LEDs are on.
7. One single digit 7-segment display
This display is connected to general purpose I/Os and can be used to display custom states/conditions. When driven low, corresponding segments are on.

Connectors, Board-to-Board

The DIGILAB megAPEX supports a high number of I/Os for data input and output as well as board to board connections. The basic signal path is meant to be from left to right which is also reflected in the naming conventions. A restriction only applies to LVDS signals which are strictly left to right for board to board or bottom to top for direct inputs/outputs. All other I/Os can be inputs/outputs or bi-directional ports and therefore signals can drive in any direction. The following basic signal paths are available:

1. Board-to-Board

There are 77 board to board signals on each side of the module. The recommended I/O standard for these signals is LVCMOS or LVTTTL. The PCI I/O option which activates a clamping diode inside the APEX I/O pin can be used to minimize overshoots. When two modules are connected together half of the signals (e.g. 0..39) can be accessed on one side of the module-to-module connection while the other half of the signals (e.g. 40..79) are accessible on the other side. The same applies if there's a termination module connected.

2. Ultra Fast Common Bus (GTL+)

There's a 48 bit common bus between all modules. The primary intent of this bus is the distribution of control signals to all modules in the system. Every single bit can be used in either LVTTTL, LVCMOS or GTL+ mode.

Furthermore each bit of this bus can represent a point-to-point, single-driver-multi-drop or multi-driver-multi-drop connection. For GTL+ mode the termination modules need to be used on both sides of the system equipped with termination resistors for each signal in GTL+ mode.

GTL+ is an open drain standard which allows the implementation of wired AND functions. This e.g. can be used efficiently to distribute a global reset over multiple modules. Through the use of bi-directional open drain ports driving the same net each module can drive and sense a global reset.

Note: The following two rules limit the number of output or bi-directional signals that can be simultaneously used in GTL+ mode in the Ultra Fast Common bus on a given logic module:

- a. All output drivers between two GNDIO pins must sink a total current of 273mA or less. The current requirement for I/O standards with a 3.3-V VCCIO level is defined as follows:

$$\begin{aligned} & ((\text{<number of GTL+>} \times 36) + (\text{<number of LVTTTL>} \times \text{ILVTTL}) + \\ & (\text{<number of PCI>} \times 1.5) + (\text{<number of LVCMOS>} \times \text{ILVCMOS}) + \\ & (\text{<number of SSTL-3 class I>} \times 8) + \\ & (\text{<number of SSTL-3 class II>} \times 16) + (\text{<number of LVDS>} \times 4.5) + \\ & (\text{<number of AGP>} \times 1.5) + (\text{<number of CTT>} \times 8)) \text{ mA} \leq 273\text{mA} \end{aligned}$$

Where ILVTTL (4 mA default value) and ILVCMOS (0.1 mA default value) are the current sink on the LVTTTL and LVCMOS pins, respectively.

- b. You cannot place output or bi-directional pins to a location that is too close to a VREF pin. Output or bi-directional pins must not be placed within two pads of a VREF pin.

3. Board-to-Board LVDS

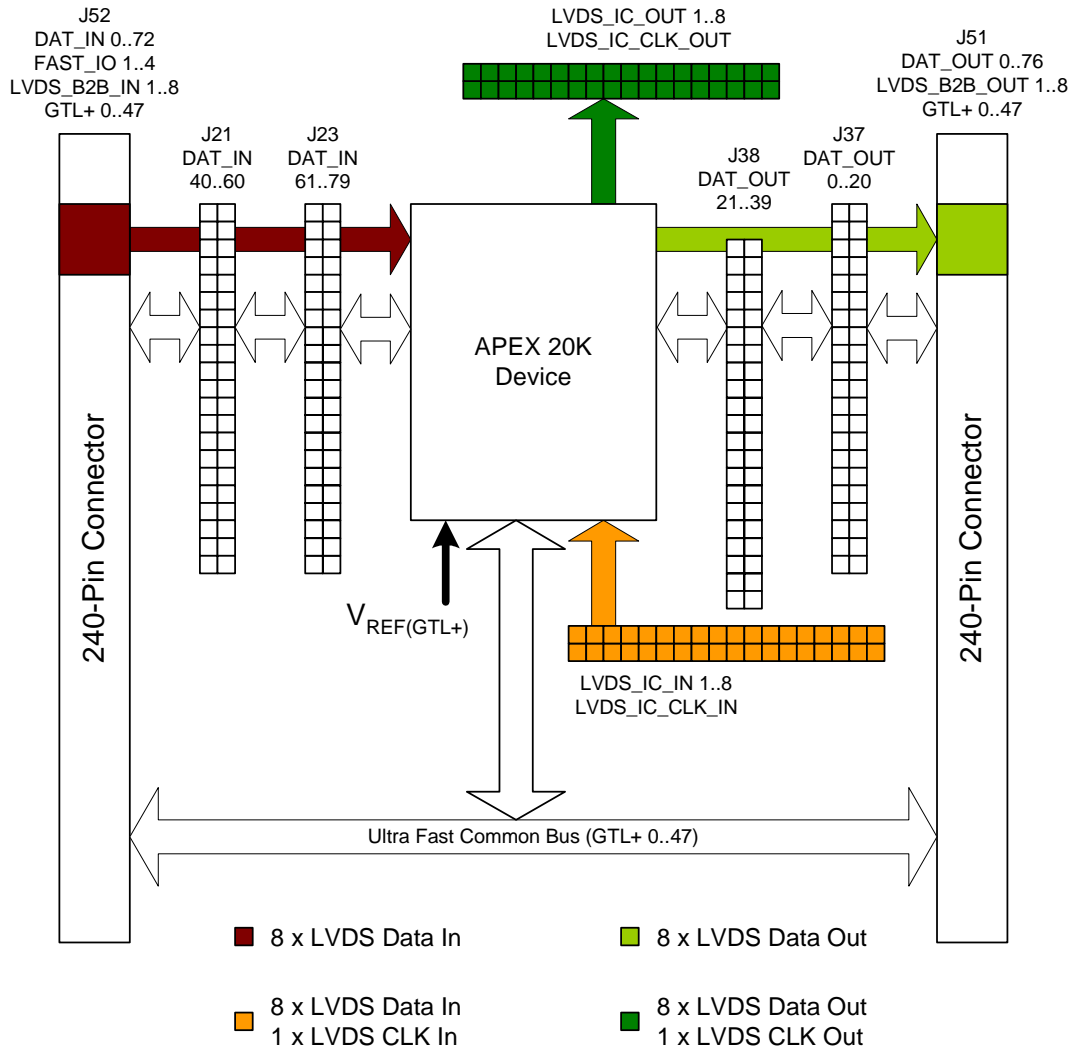
There are 8 LVDS inputs on the left side and 8 LVDS outputs on the right side of each module. These LVDS signals can only be used for board-to-board connections or be accessed on the termination modules. Since there's no clock directly associated with these connection a global system clock generated by one master module and distributed to all sub-modules needs to be used. When not used in LVDS mode these signals may also be used as standard I/Os. In this case however some limitations apply due to the 100 Ohm termination on the input side.

4. Direct LVDS in/out

There are 8 LVDS input and 8 LVDS output channels accompanied by input and output clocks on each module. These channels are meant for high speed data injection or output. When not used in LVDS mode the signals may be used as standard I/Os. In this case however some limitations apply due to the 100 Ohm termination on the input side.

Connection	Signal	Number of Signals	
		Standard	Special
Board-to-Board Left Side	DAT_IN 0..72	73	73
	FAST_IO 1..4	4	4
Board-to-Board Right Side	DAT_OUT 0..76	77	77
Ultra Fast Common Bus	GTL+ 0..47	48	48 (GTL+)
LVDS Board-to-Board	LVDS_B2B_IN 1..8	16 ¹	8 (LVDS)
	LVDS_B2B_OUT 1..8	16	8 (LVDS)
Direct LVDS In/Out	LVDS_IC_IN 1..8	16 ¹	8 (LVDS)
	LVDS_IC_CLK_IN	2 ¹	1 (LVDS)
	LVDS_IC_OUT 1..8	16	8 (LVDS)
	LVDS_IC_CLK_OUT	2	1 (LVDS)
Total:		270 I/Os	236 I/Os

¹ limited usage in none LVDS mode due to 100 Ohm input termination



Signal List

The following pages list all relevant megAPEX signals and how they are connected on the board. Signals that begin with “1” can be found on the Termination Out Connector while signals on the Termination In Connector are designated by a “2”.

1DAT_OUT40	J18.2 J51.181
1DAT_OUT41	J18.4 J51.183
1DAT_OUT42	J18.6 J51.184
1DAT_OUT43	J18.8 J51.186
1DAT_OUT44	J18.10 J51.187
1DAT_OUT45	J18.12 J51.189
1DAT_OUT46	J18.14 J51.190
1DAT_OUT47	J18.16 J51.192
1DAT_OUT48	J18.18 J51.193
1DAT_OUT49	J18.20 J51.195
1DAT_OUT50	J18.22 J51.196
1DAT_OUT51	J18.24 J51.198
1DAT_OUT52	J18.26 J51.199
1DAT_OUT53	J18.28 J51.201
1DAT_OUT54	J18.30 J51.202
1DAT_OUT55	J18.32 J51.204
1DAT_OUT56	J18.34 J51.205
1DAT_OUT57	J18.36 J51.207
1DAT_OUT58	J18.38 J51.208
1DAT_OUT59	J18.40 J51.149
1DAT_OUT60	J18.42 J51.150
1DAT_OUT61	J19.42 J51.152
1DAT_OUT62	J19.40 J51.153
1DAT_OUT63	J19.38 J51.155
1DAT_OUT64	J19.36 J51.156
1DAT_OUT65	J19.34 J51.158
1DAT_OUT66	J19.32 J51.159
1DAT_OUT67	J19.30 J51.161
1DAT_OUT68	J19.28 J51.162
1DAT_OUT69	J19.26 J51.164
1DAT_OUT70	J19.24 J51.165
1DAT_OUT71	J19.22 J51.167
1DAT_OUT72	J19.20 J51.168
1DAT_OUT73	J19.18 J51.170
1DAT_OUT74	J19.16 J51.171
1DAT_OUT75	J19.14 J51.173
1DAT_OUT76	J19.12 J51.174
1GTL+0	J43.2 J51.86 RN100.2
1GTL+1	J43.4 J51.88 RN100.4
1GTL+2	J43.6 J51.90 RN100.6
1GTL+3	J43.8 J51.92 RN100.8
1GTL+4	J43.10 J51.94 RN101.2
1GTL+5	J43.12 J51.96 RN101.4
1GTL+6	J43.14 J51.98 RN101.6
1GTL+7	J43.16 J51.100 RN101.8
1GTL+8	J43.18 J51.102 RN102.2
1GTL+9	J43.20 J51.104 RN102.4
1GTL+10	J43.22 J51.106 RN102.6
1GTL+11	J43.24 J51.108 RN102.8
1GTL+12	J43.26 J51.110 RN103.2
1GTL+13	J43.28 J51.112 RN103.4
1GTL+14	J43.30 J51.114 RN103.6
1GTL+15	J43.32 J51.116 RN103.8
1GTL+16	J43.34 J51.118 RN104.8
1GTL+17	J43.36 J51.120 RN104.2
1GTL+18	J42.42 J51.121 RN104.4
1GTL+19	J42.40 J51.123 RN104.6
1GTL+20	J42.38 J51.125 RN107.8
1GTL+21	J42.36 J51.127 RN107.6
1GTL+22	J42.34 J51.129 RN107.4

1GTL+23	J42.32 J51.131 RN107.2
1GTL+24	J42.30 J51.133 RN106.8
1GTL+25	J42.28 J51.135 RN106.6
1GTL+26	J42.26 J51.137 RN106.4
1GTL+27	J42.24 J51.139 RN106.2
1GTL+28	J42.22 J51.141 RN105.8
1GTL+29	J42.20 J51.143 RN105.6
1GTL+30	J42.18 J51.145 RN105.4
1GTL+31	J42.16 J51.147 RN105.2
1GTL+32	J41.2 J51.210 RN108.2
1GTL+33	J41.4 J51.212 RN108.4
1GTL+34	J41.6 J51.214 RN108.6
1GTL+35	J41.8 J51.216 RN108.8
1GTL+36	J41.10 J51.218 RN109.2
1GTL+37	J41.12 J51.220 RN109.4
1GTL+38	J41.14 J51.222 RN109.6
1GTL+39	J41.16 J51.224 RN109.8
1GTL+40	J41.18 J51.226 RN110.2
1GTL+41	J41.20 J51.228 RN110.4
1GTL+42	J41.22 J51.230 RN110.6
1GTL+43	J41.24 J51.232 RN110.8
1GTL+44	J41.26 J51.234 RN111.2
1GTL+45	J41.28 J51.236 RN111.4
1GTL+46	J41.30 J51.238 RN111.6
1GTL+47	J41.32 J51.240 RN111.8
1LVDS_B2B_OUT1+	J39.6 J51.62
1LVDS_B2B_OUT1-	J39.8 J51.63
1LVDS_B2B_OUT2+	J39.12 J51.66
1LVDS_B2B_OUT2-	J39.10 J51.65
1LVDS_B2B_OUT3+	J39.14 J51.68
1LVDS_B2B_OUT3-	J39.16 J51.69
1LVDS_B2B_OUT4+	J39.20 J51.72
1LVDS_B2B_OUT4-	J39.18 J51.71
1LVDS_B2B_OUT5+	J39.22 J51.74
1LVDS_B2B_OUT5-	J39.24 J51.75
1LVDS_B2B_OUT6+	J39.28 J51.78
1LVDS_B2B_OUT6-	J39.26 J51.77
1LVDS_B2B_OUT7+	J39.30 J51.80
1LVDS_B2B_OUT7-	J39.32 J51.81
1LVDS_B2B_OUT8+	J39.36 J51.84
1LVDS_B2B_OUT8-	J39.34 J51.83
1_8V_CLK	CA102.2 CA103.2 CP101.1 FB100.1 U1.AA35 U1.T34
1_8V_CLK_B	CA104.2 CA105.2 CP104.1 CP105.1 FB103.1 U1.R4 U1.W4
2DAT_IN0	J31.2 J52.60
2DAT_IN1	J31.4 J52.58
2DAT_IN2	J31.6 J52.57
2DAT_IN3	J31.8 J52.55
2DAT_IN4	J31.10 J52.54
2DAT_IN5	J31.12 J52.52
2DAT_IN6	J31.14 J52.51
2DAT_IN7	J31.16 J52.49
2DAT_IN8	J31.18 J52.48
2DAT_IN9	J31.20 J52.46
2DAT_IN10	J31.22 J52.45
2DAT_IN11	J31.24 J52.43
2DAT_IN12	J31.26 J52.42
2DAT_IN13	J31.28 J52.40
2DAT_IN14	J31.30 J52.39
2DAT_IN15	J31.32 J52.37
2DAT_IN16	J31.34 J52.36
2DAT_IN17	J31.36 J52.34
2DAT_IN18	J31.38 J52.33
2DAT_IN19	J31.40 J52.31
2DAT_IN20	J31.42 J52.30
2DAT_IN21	J30.2 J52.28
2DAT_IN22	J30.4 J52.27
2DAT_IN23	J30.6 J52.25
2DAT_IN24	J30.8 J52.24
2DAT_IN25	J30.10 J52.22
2DAT_IN26	J30.12 J52.21
2DAT_IN27	J30.14 J52.19
2DAT_IN28	J30.16 J52.18

2DAT_IN29	J30.18 J52.16
2DAT_IN30	J30.20 J52.15
2DAT_IN31	J30.22 J52.13
2DAT_IN32	J30.24 J52.12
2DAT_IN33	J30.26 J52.10
2DAT_IN34	J30.28 J52.9
2DAT_IN35	J30.30 J52.7
2DAT_IN36	J30.32 J52.6
2DAT_IN37	J30.34 J52.4
2DAT_IN38	J30.36 J52.3
2DAT_IN39	J30.38 J52.1
2GTL+0	J44.2 J52.86 RN123.2
2GTL+1	J44.4 J52.88 RN123.4
2GTL+2	J44.6 J52.90 RN123.6
2GTL+3	J44.8 J52.92 RN123.8
2GTL+4	J44.10 J52.94 RN122.2
2GTL+5	J44.12 J52.96 RN122.4
2GTL+6	J44.14 J52.98 RN122.6
2GTL+7	J44.16 J52.100 RN122.8
2GTL+8	J44.18 J52.102 RN121.2
2GTL+9	J44.20 J52.104 RN121.4
2GTL+10	J44.22 J52.106 RN121.6
2GTL+11	J44.24 J52.108 RN121.8
2GTL+12	J44.26 J52.110 RN120.2
2GTL+13	J44.28 J52.112 RN120.4
2GTL+14	J44.30 J52.114 RN120.6
2GTL+15	J44.32 J52.116 RN120.8
2GTL+16	J44.34 J52.118 RN119.8
2GTL+17	J44.36 J52.120 RN119.2
2GTL+18	J45.42 J52.121 RN119.4
2GTL+19	J45.40 J52.123 RN119.6
2GTL+20	J45.38 J52.125 RN116.8
2GTL+21	J45.36 J52.127 RN116.6
2GTL+22	J45.34 J52.129 RN116.4
2GTL+23	J45.32 J52.131 RN116.2
2GTL+24	J45.30 J52.133 RN117.8
2GTL+25	J45.28 J52.135 RN117.6
2GTL+26	J45.26 J52.137 RN117.4
2GTL+27	J45.24 J52.139 RN117.2
2GTL+28	J45.22 J52.141 RN118.8
2GTL+29	J45.20 J52.143 RN118.6
2GTL+30	J45.18 J52.145 RN118.4
2GTL+31	J45.16 J52.147 RN118.2
2GTL+32	J46.2 J52.210 RN115.2
2GTL+33	J46.4 J52.212 RN115.4
2GTL+34	J46.6 J52.214 RN115.6
2GTL+35	J46.8 J52.216 RN115.8
2GTL+36	J46.10 J52.218 RN114.2
2GTL+37	J46.12 J52.220 RN114.4
2GTL+38	J46.14 J52.222 RN114.6
2GTL+39	J46.16 J52.224 RN114.8
2GTL+40	J46.18 J52.226 RN113.2
2GTL+41	J46.20 J52.228 RN113.4
2GTL+42	J46.22 J52.230 RN113.6
2GTL+43	J46.24 J52.232 RN113.8
2GTL+44	J46.26 J52.234 RN112.2
2GTL+45	J46.28 J52.236 RN112.4
2GTL+46	J46.30 J52.238 RN112.6
2GTL+47	J46.32 J52.240 RN112.8
2LVDS_B2B_IN1+	J40.6 J52.62
2LVDS_B2B_IN1-	J40.8 J52.63
2LVDS_B2B_IN2+	J40.12 J52.66
2LVDS_B2B_IN2-	J40.10 J52.65
2LVDS_B2B_IN3+	J40.14 J52.68
2LVDS_B2B_IN3-	J40.16 J52.69
2LVDS_B2B_IN4+	J40.20 J52.72
2LVDS_B2B_IN4-	J40.18 J52.71
2LVDS_B2B_IN5+	J40.22 J52.74
2LVDS_B2B_IN5-	J40.24 J52.75
2LVDS_B2B_IN6+	J40.28 J52.78
2LVDS_B2B_IN6-	J40.26 J52.77
2LVDS_B2B_IN7+	J40.30 J52.80

2LVDS_B2B_IN7-	J40.32 J52.81
2LVDS_B2B_IN8+	J40.36 J52.84
2LVDS_B2B_IN8-	J40.34 J52.83
3_3V	CA152.2 CA153.2 CA154.2 CA155.2 CA196.2 CA197.2 CA198.2 CA200.2 CA201.2 CA202.2 CA203.2 CA205.2 CA206.2 CA207.2 CA208.2 CA209.2 CA210.2 CA212.2 CA213.2 CA214.2 CA216.2 CA217.2 CA218.2 CA219.2 CA220.2 CA221.2 CA222.2 CA223.2 CA224.2 CA225.2 CA226.2 CA227.2 CA228.2 CA229.2 CA230.2 CA231.2 CA232.2 CA233.2 CA234.2 CA235.2 CA236.2 CA237.2 CA239.2 CP100.1 CP118.1 D1.2 D2.2 D3.2 D4.2 FB118.1 FB119.1 J8.3 J8.8 J23.4 J24.4 J24.6 J25.4 J38.40 J49.175 J49.176 J49.177 J50.178 J50.179 J50.180 R3.2 R5.2 R7.3 R8.3 R9.2 R10.2 R11.2 R12.2 R13.2 R14.2 R15.2 R22.3 R23.3 R40.3 R42.2 R43.2 R44.2 R53.2 R54.2 R55.2 R56.2 R57.2 R58.2 R59.2 R60.2 R61.2 R62.2 R63.2 R64.2 R65.2 R66.2 R67.2 R79.2 R81.2 R84.1 R85.1 U1.AL3 U1.AL4 U1.AL17 U1.AL19 U1.AL31 U1.AL32 U1.AM5 U1.AN4 U1.AN32 U1.AN33 U1.C4 U1.C32 U1.D5 U1.D31 U1.E3 U1.E4 U1.E17 U1.E19 U1.F30 U1.F31 U1.U6 U1.U30 U1.U33 U1.W6 U1.W30 U1.Y1 U5.37 U5.47 U6.37 U6.47 U7.16 U8.2 U8.14 U8.23 U8.29 U8.50 U9.2 U9.14 U9.23 U9.29 U9.50 U10.3 U11.3 U14.1 U14.2 U14.3 U15.A2 U15.D6 U15.D9 U15.D10 U15.E4 U15.E7 U15.G1 U15.G10
3_3V1	CA119.2 CP112.1 J51.178 J51.179 J51.180 U4.VI
3_3V2	CA110.2 CP102.1 J52.175 J52.176 J52.177 U20.VI
7SEG_A	R76.2 U1.G4
7SEG_B	R75.2 U1.G3
7SEG_C	R73.1 U1.F2
7SEG_D	R72.1 U1.E1
7SEG_DP	R74.1 U1.H3
7SEG_E	R71.1 U1.G2
7SEG_F	R78.2 U1.H6
7SEG_G	R77.2 U1.H4
A2	U1.AE34 U5.25 U6.25 U8.11 U9.11
A3	U1.AE35 U5.24 U6.24 U8.10 U9.10
A4	U1.AD30 U5.23 U6.23 U8.9 U9.9
A5	U1.AD31 U5.22 U6.22 U8.8 U9.8
A6	U1.AD32 U5.21 U6.21 U8.7 U9.7
A7	U1.AD33 U5.20 U6.20 U8.48 U9.48
A8	U1.AD34 U5.19 U6.19 U8.47 U9.47
A9	U1.AD35 U5.18 U6.18 U8.46 U9.46
A10	U1.AC30 U5.8 U6.8 U8.45 U9.45
A11	U1.AC31 U5.7 U6.7 U8.44 U9.44
A12	U1.AC33 U5.6 U6.6 U8.38 U9.38
A13	U1.AC34 U5.5 U6.5 U8.37 U9.37
A14	U1.AC35 U5.4 U6.4 U8.36 U9.36
A15	U1.AB30 U5.3 U6.3 U8.35 U9.35
A16	U1.AB31 U5.2 U6.2 U8.34 U9.34
A17	U1.AB32 U5.1 U6.1 U8.21 U9.21
A18	U1.AB33 U5.48 U6.48 U8.20 U9.20
A19	U1.AB34 U5.17 U6.17 U8.19 U9.19
A20	U1.AB35 U5.16 U6.16 U8.18 U9.18
A21	U1.AA32 U5.9 U6.9 U8.17 U9.17
A22	U1.AA33 U5.10 U6.10
A23	U1.AA34 U5.13 U6.13
CLK1N	J1.4 R88.2 U1.Y33
CLK1P	J1.2 R88.1 U1.Y34
CLK_LVDS1N	J7.3 U17.36
CLK_LVDS1P	J7.1 U17.37
CLK_LVDS2N	J6.3 U17.34
CLK_LVDS2P	J6.1 U17.35
CLK_LVDS3N	J5.3 U17.32
CLK_LVDS3P	J5.1 U17.33
CLK_LVDS4N	J4.3 U17.30
CLK_LVDS4P	J4.1 U17.31
CLK_LVDS5N	J32.3 U17.28
CLK_LVDS5P	J32.1 U17.29
CLK_LVDS6N	J33.3 U17.26
CLK_LVDS6P	J33.1 U17.27
CLK_REF1_MP	R24.3 U1.Y3
CLK_REF2_MN	U1.T35 U17.11
CLK_REF2_MP	U1.U31 U17.10
CLK_REFERENCE	R52.2 U1.U2 U1.W34
CLK_Y1	J9.1 R45.2
CLK_Y2	J10.1 R46.2
CLK_Y3	J11.1 R48.2
CLK_Y4	J12.1 R47.2
CLK_Y5	J13.1 R50.2

CLK_Y6	J27.1 R49.2
CONFDONE	J24.3 R44.1 TP100.1 U1.AM17 U10.4 U15.G2
CTS_TX2	FB101.1 U7.7
CTS_MPX232	U1.F5 U7.9
DATA_CONF	J28.3 U15.G12
DATA_CONF_0	J24.9 J28.4 R9.1 U1.U4
DAT_IN0	J49.60 U1.AL7
DAT_IN1	J49.58 U1.AM6
DAT_IN2	J49.57 U1.AP3
DAT_IN3	J49.55 U1.AN5
DAT_IN4	J49.54 U1.AR2
DAT_IN5	J49.52 U1.AP4
DAT_IN6	J49.51 U1.AL8
DAT_IN7	J49.49 U1.AM7
DAT_IN8	J49.48 U1.AN6
DAT_IN9	J49.46 U1.AR3
DAT_IN10	J49.45 U1.AP5
DAT_IN11	J49.43 U1.AL9
DAT_IN12	J49.42 U1.AR4
DAT_IN13	J49.40 U1.AM8
DAT_IN14	J49.39 U1.AN7
DAT_IN15	J49.37 U1.AP6
DAT_IN16	J49.36 U1.AR5
DAT_IN17	J49.34 U1.AM9
DAT_IN18	J49.33 U1.AL10
DAT_IN19	J49.31 U1.AN8
DAT_IN20	J49.30 U1.AP7
DAT_IN21	J49.28 U1.AR6
DAT_IN22	J49.27 U1.AM10
DAT_IN23	J49.25 U1.AN9
DAT_IN24	J49.24 U1.AL11
DAT_IN25	J49.22 U1.AP8
DAT_IN26	J49.21 U1.AR7
DAT_IN27	J49.19 U1.AM11
DAT_IN28	J49.18 U1.AN10
DAT_IN29	J49.16 U1.AP9
DAT_IN30	J49.15 U1.AR8
DAT_IN31	J49.13 U1.AN11
DAT_IN32	J49.12 U1.AP10
DAT_IN33	J49.10 U1.AR9
DAT_IN34	J49.9 U1.AL13
DAT_IN35	J49.7 U1.AM13
DAT_IN36	J49.6 U1.AN12
DAT_IN37	J49.4 U1.AP11
DAT_IN38	J49.3 U1.AL14
DAT_IN39	J49.1 U1.AR10
DAT_IN40	J21.2 J49.181 U1.AN13
DAT_IN41	J21.4 J49.183 U1.AP12
DAT_IN42	J21.6 J49.184 U1.AM14
DAT_IN43	J21.8 J49.186 U1.AR11
DAT_IN44	J21.10 J49.187 U1.AL15
DAT_IN45	J21.12 J49.189 U1.AN14
DAT_IN46	J21.14 J49.190 U1.AP13
DAT_IN47	J21.16 J49.192 U1.AR12
DAT_IN48	J21.18 J49.193 U1.AR13
DAT_IN49	J21.20 J49.195 U1.AM15
DAT_IN50	J21.22 J49.196 U1.AN15
DAT_IN51	J21.24 J49.198 U1.AL16
DAT_IN52	J21.26 J49.199 U1.AP14
DAT_IN53	J21.28 J49.201 U1.AR14
DAT_IN54	J21.30 J49.202 U1.AP15
DAT_IN55	J21.32 J49.204 U1.AR15
DAT_IN56	J21.34 J49.205 U1.AM16
DAT_IN57	J21.36 J49.207 U1.AN16
DAT_IN58	J21.38 J49.208 U1.AP16
DAT_IN59	J21.40 J49.149 U1.AR16
DAT_IN60	J21.42 J49.150 U1.L1
DAT_IN61	J23.42 J49.152 U1.M6
DAT_IN62	J23.40 J49.153 U1.M5
DAT_IN63	J23.38 J49.155 U1.M4
DAT_IN64	J23.36 J49.156 U1.M3
DAT_IN65	J23.34 J49.158 U1.M2

DAT_IN66	J23.32 J49.159 U1.M1
DAT_IN67	J23.30 J49.161 U1.N6
DAT_IN68	J23.28 J49.162 U1.N5
DAT_IN69	J23.26 J49.164 U1.N3
DAT_IN70	J23.24 J49.165 U1.N2
DAT_IN71	J23.22 J49.167 U1.N1
DAT_IN72	J23.20 J49.168 U1.P6
DAT_IN73	J23.18 U1.P5
DAT_IN74	J23.16 U1.P4
DAT_IN75	J23.14 U1.P2
DAT_IN76	J23.12 U1.P1
DAT_IN77	J23.10 U1.R6
DAT_IN78	J23.8 U1.R2
DAT_IN79	J23.6 U1.R1
DAT_OUT0	J37.2 J50.60 U1.E7
DAT_OUT1	J37.4 J50.58 U1.D6
DAT_OUT2	J37.6 J50.57 U1.B3
DAT_OUT3	J37.8 J50.55 U1.C5
DAT_OUT4	J37.10 J50.54 U1.A2
DAT_OUT5	J37.12 J50.52 U1.B4
DAT_OUT6	J37.14 J50.51 U1.E8
DAT_OUT7	J37.16 J50.49 U1.D7
DAT_OUT8	J37.18 J50.48 U1.C6
DAT_OUT9	J37.20 J50.46 U1.A3
DAT_OUT10	J37.22 J50.45 U1.B5
DAT_OUT11	J37.24 J50.43 U1.E9
DAT_OUT12	J37.26 J50.42 U1.A4
DAT_OUT13	J37.28 J50.40 U1.D8
DAT_OUT14	J37.30 J50.39 U1.C7
DAT_OUT15	J37.32 J50.37 U1.B6
DAT_OUT16	J37.34 J50.36 U1.A5
DAT_OUT17	J37.36 J50.34 U1.D9
DAT_OUT18	J37.38 J50.33 U1.E10
DAT_OUT19	J37.40 J50.31 U1.C8
DAT_OUT20	J37.42 J50.30 U1.B7
DAT_OUT21	J38.2 J50.28 U1.A26
DAT_OUT22	J38.4 J50.27 U1.E22
DAT_OUT23	J38.6 J50.25 U1.B25
DAT_OUT24	J38.8 J50.24 U1.C24
DAT_OUT25	J38.10 J50.22 U1.D23
DAT_OUT26	J38.12 J50.21 U1.E23
DAT_OUT27	J38.14 J50.19 U1.A27
DAT_OUT28	J38.16 J50.18 U1.B26
DAT_OUT29	J38.18 J50.16 U1.C25
DAT_OUT30	J38.20 J50.15 U1.A28
DAT_OUT31	J38.22 J50.13 U1.B27
DAT_OUT32	J38.24 J50.12 U1.C26
DAT_OUT33	J38.26 J50.10 U1.D25
DAT_OUT34	J38.28 J50.9 U1.A29
DAT_OUT35	J38.30 J50.7 U1.B28
DAT_OUT36	J38.32 J50.6 U1.E25
DAT_OUT37	J38.34 J50.4 U1.C27
DAT_OUT38	J38.36 J50.3 U1.D26
DAT_OUT39	J38.38 J50.1 U1.A30
DAT_OUT40	J50.181 U1.A6
DAT_OUT41	J50.183 U1.D10
DAT_OUT42	J50.184 U1.C9
DAT_OUT43	J50.186 U1.E11
DAT_OUT44	J50.187 U1.B8
DAT_OUT45	J50.189 U1.A7
DAT_OUT46	J50.190 U1.D11
DAT_OUT47	J50.192 U1.C10
DAT_OUT48	J50.193 U1.B9
DAT_OUT49	J50.195 U1.A8
DAT_OUT50	J50.196 U1.C11
DAT_OUT51	J50.198 U1.B10
DAT_OUT52	J50.199 U1.A9
DAT_OUT53	J50.201 U1.E13
DAT_OUT54	J50.202 U1.D13
DAT_OUT55	J50.204 U1.C12
DAT_OUT56	J50.205 U1.B11
DAT_OUT57	J50.207 U1.E14

DAT_OUT58 J50.208 U1.A10
 DAT_OUT59 J50.149 U1.B29
 DAT_OUT60 J50.150 U1.C28
 DAT_OUT61 J50.152 U1.E26
 DAT_OUT62 J50.153 U1.D27
 DAT_OUT63 J50.155 U1.A31
 DAT_OUT64 J50.156 U1.B30
 DAT_OUT65 J50.158 U1.C29
 DAT_OUT66 J50.159 U1.D28
 DAT_OUT67 J50.161 U1.A32
 DAT_OUT68 J50.162 U1.E27
 DAT_OUT69 J50.164 U1.B31
 DAT_OUT70 J50.165 U1.A33
 DAT_OUT71 J50.167 U1.C30
 DAT_OUT72 J50.168 U1.D29
 DAT_OUT73 J50.170 U1.E28
 DAT_OUT74 J50.171 U1.B32
 DAT_OUT75 J50.173 U1.A34
 DAT_OUT76 J50.174 U1.C31
 DCLK_CONFIG J24.1 J28.2 R10.1 U1.U3
 DEV_CLRN R59.1 TP113.1 U1.T6 U11.2
 DEV_OEN R84.2 TP112.1 U1.Y5
 DGND C2.2 C3.2 C4.2 C5.2 C7.2 CA100.1 CA101.1 CA102.1 CA103.1 CA104.1 CA105.1
 CA152.1 CA153.1 CA154.1 CA155.1 CA157.1 CA158.1 CA159.1 CA160.1 CA172.1 CA173.1
 CA174.1 CA175.1 CA176.1 CA178.1 CA179.1 CA180.1 CA181.1 CA182.1 CA183.1 CA184.1
 CA185.1 CA186.1 CA187.1 CA188.1 CA189.1 CA190.1 CA191.1 CA192.1 CA193.1 CA196.1
 CA197.1 CA198.1 CA200.1 CA201.1 CA202.1 CA203.1 CA205.1 CA206.1 CA207.1 CA208.1
 CA209.1 CA210.1 CA212.1 CA213.1 CA214.1 CA216.1 CA217.1 CA218.1 CA219.1 CA220.1
 CA221.1 CA222.1 CA223.1 CA224.1 CA225.1 CA226.1 CA227.1 CA228.1 CA229.1 CA230.1
 CA231.1 CA232.1 CA233.1 CA234.1 CA235.1 CA236.1 CA237.1 CA238.1 CA242.1 CA243.1
 CA244.1 CA245.1 CA246.1 CA247.1 CA248.1 CA249.1 CA250.1 CA251.1 CP100.2 CP101.2
 CP104.2 CP105.2 CP109.2 CP110.2 CP111.2 CP114.2 CP116.2 CP117.2 CP118.2 CP119.2
 D5.2 D6.2 J1.1 J1.3 J2.2 J2.4 J2.6 J2.8 J2.10 J2.12 J2.14 J2.16 J2.18 J2.20
 J2.22 J2.24 J2.26 J2.28 J2.30 J2.32 J2.34 J2.36 J3.1 J3.3 J3.5 J3.7 J3.9 J3.11
 J3.13 J3.15 J3.17 J3.19 J3.21 J3.23 J3.25 J3.27 J3.29 J3.31 J3.33 J3.35 J4.2
 J4.4 J5.2 J5.4 J6.2 J6.4 J7.2 J7.4 J9.2 J9.3 J9.4 J9.5 J10.2 J10.3 J10.4 J10.5
 J11.2 J11.3 J11.4 J11.5 J12.2 J12.3 J12.4 J12.5 J13.2 J13.3 J13.4 J13.5 J14.1
 J15.1 J16.1 J17.1 J20.5 J20.6 J20.7 J20.8 J21.1 J21.3 J21.5 J21.7 J21.9 J21.11
 J21.13 J21.15 J21.17 J21.19 J21.21 J21.23 J21.25 J21.27 J21.29 J21.31 J21.33
 J21.35 J21.37 J21.39 J21.41 J22.5 J23.1 J23.3 J23.5 J23.7 J23.9 J23.11 J23.13
 J23.15 J23.17 J23.19 J23.21 J23.23 J23.25 J23.27 J23.29 J23.31 J23.33 J23.35
 J23.37 J23.39 J23.41 J24.2 J24.10 J26.2 J26.3 J26.4 J26.5 J27.2 J27.3 J27.4
 J27.5 J29.1 J32.2 J32.4 J33.2 J33.4 J35.1 J35.2 J37.1 J37.3 J37.5 J37.7 J37.9
 J37.11 J37.13 J37.15 J37.17 J37.19 J37.21 J37.23 J37.25 J37.27 J37.29 J37.31
 J37.33 J37.35 J37.37 J37.39 J37.41 J38.1 J38.3 J38.5 J38.7 J38.9 J38.11 J38.13
 J38.15 J38.17 J38.19 J38.21 J38.23 J38.25 J38.27 J38.29 J38.31 J38.33 J38.35
 J38.37 J38.39 J38.41 J49.2 J49.5 J49.8 J49.11 J49.14 J49.17 J49.20 J49.23
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 MH107.1 MH108.1 R3.3 R7.2 R8.2 R17.1 R18.1 R19.1 R21.1 R22.2 R23.2 R40.2 R80.1
 SW100.3 SW100.4 SW101.3 SW101.4 SW102.3 SW102.4 SW103.3 SW103.4 U1.A1 U1.A18
 U1.A35 U1.AK18 U1.AL6 U1.AL18 U1.AL30 U1.AM2 U1.AM3 U1.AM4 U1.AM18 U1.AM31
 U1.AM32 U1.AM33 U1.AM34 U1.AN1 U1.AN2 U1.AN3 U1.AN18 U1.AN34 U1.AN35 U1.AP1
 U1.AP2 U1.AP18 U1.AP34 U1.AP35 U1.AR1 U1.AR18 U1.AR35 U1.B1 U1.B2 U1.B18 U1.B34
 U1.B35 U1.C2 U1.C3 U1.C18 U1.C33 U1.C34 U1.C35 U1.D2 U1.D3 U1.D4 U1.D17 U1.D18
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U1.R3 U1.T33 U1.U1 U1.U32 U1.U35 U1.V1 U1.V2 U1.V3 U1.V4 U1.V5 U1.V6 U1.V30
 U1.V31 U1.V32 U1.V33 U1.V34 U1.V35 U1.W2 U1.W35 U1.Y2 U1.Y30 U5.27 U5.46 U6.27
 U6.46 U7.15 U8.5 U8.26 U8.32 U8.41 U8.53 U9.5 U9.26 U9.32 U9.41 U9.53 U10.12
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 U17.3 U17.14 U17.15 U17.17 U17.19
 DGND1 CA118.1 CA119.1 CP106.2 CP112.2 CP113.2 J18.1 J18.3 J18.5 J18.7 J18.9 J18.11
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 DGND2 CA110.1 CA111.1 CP102.2 CP103.2 CP107.2 J30.1 J30.3 J30.5 J30.7 J30.9 J30.11
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 J52.227 J52.229 J52.231 J52.233 J52.235 J52.237 J52.239 U20.CON U20.GND
 DQ0 U1.AL33 U5.29 U9.22
 DQ1 U1.AK30 U5.31 U9.24
 DQ2 U1.AK31 U5.33 U9.25
 DQ3 U1.AK32 U5.35 U9.27
 DQ4 U1.AL34 U5.38 U9.28
 DQ5 U1.AM35 U5.40 U9.30
 DQ6 U1.AJ30 U5.42 U9.31
 DQ7 U1.AJ31 U5.44 U9.33
 DQ8 U1.AJ32 U5.30 U9.49
 DQ9 U1.AJ33 U5.32 U9.51
 DQ10 U1.AK34 U5.34 U9.52
 DQ11 U1.AL35 U5.36 U9.54
 DQ12 U1.AJ34 U5.39 U9.1
 DQ13 U1.AH30 U5.41 U9.3
 DQ14 U1.AH32 U5.43 U9.4
 DQ15 U1.AH33 U5.45 U9.6
 DQ16 U1.AK35 U6.29 U8.22
 DQ17 U1.AH34 U6.31 U8.24
 DQ18 U1.AJ35 U6.33 U8.25
 DQ19 U1.AG30 U6.35 U8.27
 DQ20 U1.AG31 U6.38 U8.28
 DQ21 U1.AG32 U6.40 U8.30
 DQ22 U1.AG33 U6.42 U8.31
 DQ23 U1.AG34 U6.44 U8.33
 DQ24 U1.AG35 U6.30 U8.49

DQ25	U1.AF30 U6.32 U8.51
DQ26	U1.AF31 U6.34 U8.52
DQ27	U1.AF32 U6.36 U8.54
DQ28	U1.AF33 U6.39 U8.1
DQ29	U1.AF34 U6.41 U8.3
DQ30	U1.AF35 U6.43 U8.4
DQ31	U1.AE30 U6.45 U8.6
FAST_IN1	J49.170 U1.B19
FAST_IN2	J49.171 U1.B17
FAST_IN3	J49.173 U1.AP19
FAST_IN4	J49.174 U1.AP17
GND	J25.2 J25.10 R4.1 U13.10 U13.11 U13.12 U13.13 U13.14 U13.15 U14.10 U14.11 U14.12 U14.13 U14.14 U14.15
GTL+0	J49.86 J50.86 U1.AM20
GTL+1	J49.88 J50.88 U1.AL22
GTL+2	J49.90 J50.90 U1.AN21
GTL+3	J49.92 J50.92 U1.AM21
GTL+4	J49.94 J50.94 U1.AN22
GTL+5	J49.96 J50.96 U1.AM22
GTL+6	J49.98 J50.98 U1.AN23
GTL+7	J49.100 J50.100 U1.AM23
GTL+8	J49.102 J50.102 U1.AN24
GTL+9	J49.104 J50.104 U1.AN25
GTL+10	J49.106 J50.106 U1.AM25
GTL+11	J49.108 J50.108 U1.AN26
GTL+12	J49.110 J50.110 U1.AM26
GTL+13	J49.112 J50.112 U1.AN27
GTL+14	J49.114 J50.114 U1.AN28
GTL+15	J49.116 J50.116 U1.AN29
GTL+16	J49.118 J50.118 U1.AN30
GTL+17	J49.120 J50.120 U1.AN31
GTL+18	J49.121 J50.121 U1.AP33
GTL+19	J49.123 J50.123 U1.AP32
GTL+20	J49.125 J50.125 U1.AP31
GTL+21	J49.127 J50.127 U1.AP30
GTL+22	J49.129 J50.129 U1.AP29
GTL+23	J49.131 J50.131 U1.AP28
GTL+24	J49.133 J50.133 U1.AP27
GTL+25	J49.135 J50.135 U1.AP26
GTL+26	J49.137 J50.137 U1.AP25
GTL+27	J49.139 J50.139 U1.AP24
GTL+28	J49.141 J50.141 U1.AP23
GTL+29	J49.143 J50.143 U1.AP22
GTL+30	J49.145 J50.145 U1.AP21
GTL+31	J49.147 J50.147 U1.AN20
GTL+32	J49.210 J50.210 U1.AP20
GTL+33	J49.212 J50.212 U1.AR20
GTL+34	J49.214 J50.214 U1.AR21
GTL+35	J49.216 J50.216 U1.AR22
GTL+36	J49.218 J50.218 U1.AR23
GTL+37	J49.220 J50.220 U1.AR24
GTL+38	J49.222 J50.222 U1.AR25
GTL+39	J49.224 J50.224 U1.AR26
GTL+40	J49.226 J50.226 U1.AR27
GTL+41	J49.228 J50.228 U1.AR28
GTL+42	J49.230 J50.230 U1.AR29
GTL+43	J49.232 J50.232 U1.AR30
GTL+44	J49.234 J50.234 U1.AR31
GTL+45	J49.236 J50.236 U1.AR32
GTL+46	J49.238 J50.238 U1.AR33
GTL+47	J49.240 J50.240 U1.AR34
INITDONE	R85.2 TP111.1 U1.C16 U1.W33
LED_03	U1.B16 U10.9
LED_04	U1.A16 U10.11
LVDS_B2B_IN1+	J49.62 R41.2 U1.R33
LVDS_B2B_IN1-	J49.63 R41.1 U1.R32
LVDS_B2B_IN2+	J49.66 R25.1 U1.P35
LVDS_B2B_IN2-	J49.65 R25.2 U1.R30
LVDS_B2B_IN3+	J49.68 R26.2 U1.P34
LVDS_B2B_IN3-	J49.69 R26.1 U1.P33
LVDS_B2B_IN4+	J49.72 R27.1 U1.P30
LVDS_B2B_IN4-	J49.71 R27.2 U1.P31

LVDS_B2B_IN5+	J49.74 R28.2 U1.N34
LVDS_B2B_IN5-	J49.75 R28.1 U1.N33
LVDS_B2B_IN6+	J49.78 R29.1 U1.N30
LVDS_B2B_IN6-	J49.77 R29.2 U1.N31
LVDS_B2B_IN7+	J49.80 R30.2 U1.M35
LVDS_B2B_IN7-	J49.81 R30.1 U1.M34
LVDS_B2B_IN8+	J49.84 R31.1 U1.M31
LVDS_B2B_IN8-	J49.83 R31.2 U1.M32
LVDS_B2B_OUT1+	J50.62 U1.AA5
LVDS_B2B_OUT1-	J50.63 U1.AA6
LVDS_B2B_OUT2+	J50.66 U1.AB3
LVDS_B2B_OUT2-	J50.65 U1.AB2
LVDS_B2B_OUT3+	J50.68 U1.AB4
LVDS_B2B_OUT3-	J50.69 U1.AB5
LVDS_B2B_OUT4+	J50.72 U1.AC2
LVDS_B2B_OUT4-	J50.71 U1.AC1
LVDS_B2B_OUT5+	J50.74 U1.AC4
LVDS_B2B_OUT5-	J50.75 U1.AC5
LVDS_B2B_OUT6+	J50.78 U1.AD2
LVDS_B2B_OUT6-	J50.77 U1.AD1
LVDS_B2B_OUT7+	J50.80 U1.AD3
LVDS_B2B_OUT7-	J50.81 U1.AD4
LVDS_B2B_OUT8+	J50.84 U1.AE1
LVDS_B2B_OUT8-	J50.83 U1.AD6
LVDS_IC_CLK_IN+	J2.35 R2.2 U1.T32
LVDS_IC_CLK_IN-	J2.33 R2.1 U1.T31
LVDS_IC_CLK_OUT+	J3.2 U1.W5
LVDS_IC_CLK_OUT-	J3.4 U1.Y6
LVDS_IC_IN1+	J2.31 R36.2 U1.L35
LVDS_IC_IN1-	J2.29 R36.1 U1.L34
LVDS_IC_IN2+	J2.25 R38.1 U1.L31
LVDS_IC_IN2-	J2.27 R38.2 U1.L32
LVDS_IC_IN3+	J2.23 R37.2 U1.L30
LVDS_IC_IN3-	J2.21 R37.1 U1.K35
LVDS_IC_IN4+	J2.17 R35.1 U1.K32
LVDS_IC_IN4-	J2.19 R35.2 U1.K33
LVDS_IC_IN5+	J2.15 R39.2 U1.K30
LVDS_IC_IN5-	J2.13 R39.1 U1.J35
LVDS_IC_IN6+	J2.9 R34.1 U1.J33
LVDS_IC_IN6-	J2.11 R34.2 U1.J34
LVDS_IC_IN7+	J2.7 R33.2 U1.J32
LVDS_IC_IN7-	J2.5 R33.1 U1.J31
LVDS_IC_IN8+	J2.1 R32.1 U1.H34
LVDS_IC_IN8-	J2.3 R32.2 U1.G35
LVDS_IC_OUT1+	J3.6 U1.AE3
LVDS_IC_OUT1-	J3.8 U1.AE4
LVDS_IC_OUT2+	J3.12 U1.AF1
LVDS_IC_OUT2-	J3.10 U1.AE6
LVDS_IC_OUT3+	J3.14 U1.AF2
LVDS_IC_OUT3-	J3.16 U1.AF3
LVDS_IC_OUT4+	J3.20 U1.AF6
LVDS_IC_OUT4-	J3.18 U1.AF5
LVDS_IC_OUT5+	J3.22 U1.AH1
LVDS_IC_OUT5-	J3.24 U1.AG2
LVDS_IC_OUT6+	J3.28 U1.AG5
LVDS_IC_OUT6-	J3.26 U1.AG4
LVDS_IC_OUT7+	J3.30 U1.AG6
LVDS_IC_OUT7-	J3.32 U1.AJ1
LVDS_IC_OUT8+	J3.36 U1.AH3
LVDS_IC_OUT8-	J3.34 U1.AK1
MEM_RDY_BSY	R55.1 U1.A23 U5.15 U6.15
MGPX_LOCK1	TP101.1 U1.AA30 U1.B13
MGPX_LOCK2	TP102.1 U1.A12 U1.AB6
MGPX_LOCK3	TP103.1 U1.A13 U1.R31
MGPX_LOCK4	TP104.1 U1.AC6 U1.D15
NC	J19.2 J19.4 J19.6 J19.8 J19.10 J22.1 J22.4 J22.6 J22.9 J24.8 J25.6 J25.7 J25.8 J30.40 J30.42 J39.2 J39.4 J40.2 J40.4 J41.34 J41.36 J41.38 J41.40 J41.42 J42.2 J42.4 J42.6 J42.8 J42.10 J42.12 J42.14 J43.38 J43.40 J43.42 J44.38 J44.40 J44.42 J45.2 J45.4 J45.6 J45.8 J45.10 J45.12 J45.14 J46.34 J46.36 J46.38 J46.40 J46.42 J49.178 J49.179 J49.180 J50.175 J50.176 J50.177 J51.1 J51.3 J51.4 J51.6 J51.7 J51.9 J51.10 J51.12 J51.13 J51.15 J51.16 J51.18 J51.19 J51.21 J51.22 J51.24 J51.25 J51.27 J51.28 J51.30 J51.31 J51.33 J51.34 J51.36 J51.37 J51.39

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 U1.A11 U1.A14 U1.A15 U1.A20 U1.AA1 U1.AA2 U1.AA3 U1.AB1 U1.AD5 U1.AE5 U1.AE31
 U1.AE32 U1.AF4 U1.AG3 U1.AH2 U1.AH5 U1.AH6 U1.AJ2 U1.AJ3 U1.AJ4 U1.AJ5 U1.AJ6
 U1.AK2 U1.AK3 U1.AK4 U1.AK5 U1.AK6 U1.AL1 U1.AL26 U1.AL27 U1.AL28 U1.AL29
 U1.AM1 U1.AM27 U1.AM29 U1.B12 U1.B14 U1.B15 U1.B20 U1.B24 U1.B33 U1.C13 U1.C14
 U1.C15 U1.C19 U1.C20 U1.C23 U1.D14 U1.D16 U1.D20 U1.D30 U1.D35 U1.E15 U1.E16
 U1.E29 U1.E34 U1.E35 U1.F32 U1.F33 U1.F34 U1.G31 U1.G32 U1.G33 U1.G34 U1.H30
 U1.H31 U1.H32 U1.H33 U1.H35 U1.J1 U1.J2 U1.J3 U1.J4 U1.J5 U1.J6 U1.J30 U1.K1
 U1.K2 U1.K3 U1.K4 U1.K5 U1.K6 U1.K34 U1.L2 U1.L4 U1.L5 U1.L6 U1.L33 U1.M33
 U1.N32 U1.P32 U1.R35 U1.T3 U1.T30 U1.Y4 U8.16 U8.40 U8.43 U9.16 U9.40 U9.43
 U12.2 U12.4 U12.9 U15.A1 U15.A3 U15.A4 U15.A5 U15.A6 U15.A7 U15.A8 U15.A11
 U15.A12 U15.B3 U15.B4 U15.B5 U15.B6 U15.B7 U15.B9 U15.B10 U15.B11 U15.B12
 U15.C4 U15.C7 U15.C8 U15.C9 U15.C10 U15.C11 U15.D7 U15.D11 U15.E5 U15.E6 U15.E8
 U15.E9 U15.E10 U15.E11 U15.F3 U15.F4 U15.F7 U15.F8 U15.F9 U15.F10 U15.F11
 U15.G3 U15.G4 U15.G5 U15.G6 U15.G7 U15.G8 U15.G9 U15.H1 U15.H4 U15.H5 U15.H6
 U15.H7 U15.H9 U15.H12 U16.1 U16.2 U16.7 U16.8 U17.4 U17.16 U17.20 U17.21 U17.22
 U17.23 U17.24 U17.25 U17.38
 J24.5 J28.8 R42.1 U1.W32
 J24.7 J28.6 R43.1 U1.AN17 U10.7
 J28.5 J29.2 U15.B1
 J16.2 Q1.B R83.1
 J17.2 Q2.B R82.1
 FB102.1 U7.7
 U1.F6 U7.10
 FB111.2 U7.13
 U1.C1 U7.12
 C1.1 C6.2 C8.1 C9.2 J36.1 J36.2
 J20.1 R63.1 U1.D1
 J20.2 R62.1 U1.E2
 J20.3 R61.1 U1.G6
 J20.4 R60.1 U1.G5
 R58.1 U1.G1 U11.13
 R57.1 U1.F1 U11.1
 R11.1 U1.H2 U11.14
 J25.1 R13.1 R17.2 U1.AN19 U15.C2
 J25.9 R15.1 R16.2 U15.D2
 J25.3 R1.1
 J25.5 R14.1 U1.AM19 U15.F2
 J15.2 R12.1 U1.D19
 FB112.2 U7.14
 U1.F4 U7.11
 R4.2 R5.1 U10.5 U10.6 U10.8 U10.10 U11.4 U11.6 U11.8 U11.10
 CA100.2 CA247.2 CA248.2 CA249.2 CP110.1 FB118.2 U12.3 U12.10 U12.15 U12.22
 CA250.2 CA251.2 CP111.1 FB119.2 U17.2 U17.5 U17.6 U17.7 U17.8 U17.9 U17.12
 U17.13 U17.18
 CP117.1 D5.1 F1.2 FB117.1 J23.2 J38.42 Q1.E Q2.E R82.2 R83.2 U13.6 U13.7 U14.6
 U14.7
 CA157.2 CA158.2 CA159.2 CA160.2 CA172.2 CA173.2 CA174.2 CA175.2 CA176.2 CA178.2
 CA179.2 CA180.2 CA181.2 CA182.2 CA183.2 CA184.2 CA185.2 CA186.2 CA187.2 CA188.2
 CA189.2 CA190.2 CA191.2 CA192.2 CA193.2 CP116.1 CP119.1 FB100.2 FB103.2 R20.2
 U1.A17 U1.A19 U1.AA4 U1.AA31 U1.AC3 U1.AC32 U1.AE2 U1.AE33 U1.AG1 U1.AH4
 U1.AH31 U1.AH35 U1.AK33 U1.AL12 U1.AL24 U1.AM12 U1.AM24 U1.AR17 U1.AR19 U1.D12
 U1.D24 U1.E12 U1.E24 U1.F3 U1.F35 U1.G30 U1.H1 U1.H5 U1.K31 U1.L3 U1.M30 U1.N4
 U1.N35 U1.R5 U1.R34 U1.U5 U1.U34 U1.W3 U1.W31 U13.1 U13.2 U13.3
 CA246.2 CP109.1 FB117.2 U16.5 U16.6
 CA242.2 CA243.2 CA244.2 CA245.2 CP114.1 R79.1 R80.2 U1.AL20 U1.AL21 U1.AL23
 U1.AL25 U1.AM28 U1.AM30
 CA118.2 CP106.1 CP113.1 J47.1 J47.2 RN100.1 RN100.3 RN100.5 RN100.7 RN101.1
 RN101.3 RN101.5 RN101.7 RN102.1 RN102.3 RN102.5 RN102.7 RN103.1 RN103.3 RN103.5
 RN103.7 RN104.1 RN104.3 RN104.5 RN104.7 RN105.1 RN105.3 RN105.5 RN105.7 RN106.1
 RN106.3 RN106.5 RN106.7 RN107.1 RN107.3 RN107.5 RN107.7 RN108.1 RN108.3 RN108.5
 RN108.7 RN109.1 RN109.3 RN109.5 RN109.7 RN110.1 RN110.3 RN110.5 RN110.7 RN111.1
 RN111.3 RN111.5 RN111.7 U4.VO
 CA111.2 CP103.1 CP107.1 J48.1 J48.2 RN112.1 RN112.3 RN112.5 RN112.7 RN113.1
 RN113.3 RN113.5 RN113.7 RN114.1 RN114.3 RN114.5 RN114.7 RN115.1 RN115.3 RN115.5
 RN115.7 RN116.1 RN116.3 RN116.5 RN116.7 RN117.1 RN117.3 RN117.5 RN117.7 RN118.1
 RN118.3 RN118.5 RN118.7 RN119.1 RN119.3 RN119.5 RN119.7 RN120.1 RN120.3 RN120.5

NCONFIG
 NSTATUS
 NSTATUS_SW
 POWER_SWITCH1
 POWER_SWITCH2
 RTS_RX2
 RTS_MPX232
 RX
 RX_MPX232
 SGND
 SW_JMP1
 SW_JMP2
 SW_JMP3
 SW_JMP4
 SW_PB2
 SW_PB3
 SW_PB4
 TCK
 TDI_JTAG_MAIN
 TDO
 TMS
 TRST
 TX
 TX_MPX232
 VCCINT_REF
 VCC_CLK
 VCC_CLK_LVDS
 VDD
 VDD1_8
 VDD_OSZ
 VREF
 VTT1
 VTT2

	RN120.7 RN121.1 RN121.3 RN121.5 RN121.7 RN122.1 RN122.3 RN122.5 RN122.7 RN123.1 RN123.3 RN123.5 RN123.7 U20.VO
~BEN_0	U1.B22 U9.39
~BEN_1	U1.A22 U9.12
~BEN_2	U1.B21 U8.39
~BEN_3	U1.A21 U8.12
~MEM_CE	R54.1 U1.E20 U8.13 U9.13
~MEM_FH_CE	R56.1 U1.A24 U6.26
~MEM_FL_CE	R53.1 U1.D22 U5.26
~MEM_F_OE	U1.E21 U5.28 U6.28
~MEM_F_RESET	U1.B23 U5.12 U6.12
~MEM_F_WE	U1.A25 U5.11 U6.11
~MEM_F_WP	U1.C22 U5.14 U6.14
~MEM_OE	U1.D21 U8.42 U9.42
~MEM_WE	U1.C21 U8.15 U9.15

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Version V01

7
6
5
4
3
2
1

Order of the Sheets

- 1 Top Sheet
- 2 Connector In
- 3 Connector Out
- 4 megAPEX Standard IO I
- 5 megAPEX Standard IO II
- 6 megAPEX SYM IO
- 7 megAPEX CONF, JTAG
- 8 megAPEX Power
- 9 Memory
- 10 RS232, Switch, LED
- 11 Power, Mechanics
- 12 CLK Tree
- 13 Connector Termination Out
- 14 Connector Termination In

DESIGN definitions

El Camino GmbH

Title	
megAPEX Top Sheet	
Document Name	Author
MGPX_V01	FH
Date	Sheet
3-23-2001_13:17	1

A B C D E F G H I J

DAT_IN39	DGND	149
DAT_IN38	DGND	181
DAT_IN37	DGND	182
DAT_IN36	DGND	183
DAT_IN35	DGND	184
DAT_IN34	DGND	185
DAT_IN33	DGND	186
DAT_IN32	DGND	187
DAT_IN31	DGND	188
DAT_IN30	DGND	189
DAT_IN29	DGND	190
DAT_IN28	DGND	191
DAT_IN27	DGND	192
DAT_IN26	DGND	193
DAT_IN25	DGND	194
DAT_IN24	DGND	195
DAT_IN23	DGND	196
DAT_IN22	DGND	197
DAT_IN21	DGND	198
DAT_IN20	DGND	199
DAT_IN19	DGND	200
DAT_IN18	DGND	201
DAT_IN17	DGND	202
DAT_IN16	DGND	203
DAT_IN15	DGND	204
DAT_IN14	DGND	205
DAT_IN13	DGND	206
DAT_IN12	DGND	207
DAT_IN11	DGND	208
DAT_IN10	DGND	209
DAT_IN9	DGND	210
DAT_IN8	DGND	211
DAT_IN7	DGND	212
DAT_IN6	DGND	213
DAT_IN5	DGND	214
DAT_IN4	DGND	215
DAT_IN3	DGND	216
DAT_IN2	DGND	217
DAT_IN1	DGND	218
DAT_IN0	DGND	219

IO1

DEVICE=HD90_240F
 PARTS=STD
 PRG TYPE=HD90_240F
 HD90_240F_IO1,HD90_240F_IO2,HD90_240F_IO3,HD90_240F_IO4
 HETERO_SYMNAME=HD90_240F_IO1

LVDS_B2B_IN1+	DGND	61
LVDS_B2B_IN1-	DGND	62
LVDS_B2B_IN2-	DGND	63
LVDS_B2B_IN2+	DGND	64
LVDS_B2B_IN3+	DGND	65
LVDS_B2B_IN3-	DGND	66
LVDS_B2B_IN4-	DGND	67
LVDS_B2B_IN4+	DGND	68
LVDS_B2B_IN5+	DGND	69
LVDS_B2B_IN5-	DGND	70
LVDS_B2B_IN6-	DGND	71
LVDS_B2B_IN6+	DGND	72
LVDS_B2B_IN7+	DGND	73
LVDS_B2B_IN7-	DGND	74
LVDS_B2B_IN8-	DGND	75
LVDS_B2B_IN8+	DGND	76
GTL+0	DGND	77
GTL+1	DGND	78
GTL+2	DGND	79
GTL+3	DGND	80
GTL+4	DGND	81
GTL+5	DGND	82
GTL+6	DGND	83
GTL+7	DGND	84
GTL+8	DGND	85
GTL+9	DGND	86
GTL+10	DGND	87
GTL+11	DGND	88
GTL+12	DGND	89
GTL+13	DGND	90
GTL+14	DGND	91
GTL+15	DGND	92
GTL+16	DGND	93
GTL+17	DGND	94

IO2

SYM

DEVICE=HD90_240F
 PARTS=STD
 PRG TYPE=HD90_240F
 HETERO=HD90_240F_IO1,HD90_240F_IO2,HD90_240F_IO3,HD90_240F_IO4
 HETERO_SYMNAME=HD90_240F_IO2

GTL+18	DGND	121
GTL+19	DGND	122
GTL+20	DGND	123
GTL+21	DGND	124
GTL+22	DGND	125
GTL+23	DGND	126
GTL+24	DGND	127
GTL+25	DGND	128
GTL+26	DGND	129
GTL+27	DGND	130
GTL+28	DGND	131
GTL+29	DGND	132
GTL+30	DGND	133
GTL+31	DGND	134
DAT_IN59	DGND	149
DAT_IN60	DGND	150
DAT_IN61	DGND	151
DAT_IN62	DGND	152
DAT_IN63	DGND	153
DAT_IN64	DGND	154
DAT_IN65	DGND	155
DAT_IN66	DGND	156
DAT_IN67	DGND	157
DAT_IN68	DGND	158
DAT_IN69	DGND	159
DAT_IN70	DGND	160
DAT_IN71	DGND	161
DAT_IN72	DGND	162
FAST_IN1	DGND	163
FAST_IN2	DGND	164
FAST_IN3	DGND	165
FAST_IN4	DGND	166
3.3V	DGND	167
3.3V	DGND	168
3.3V	DGND	169
NC	DGND	170
NC	DGND	171
NC	DGND	172
NC	DGND	173
NC	DGND	174
NC	DGND	175
NC	DGND	176
NC	DGND	177
NC	DGND	178
NC	DGND	179
NC	DGND	180

IO3

SYM

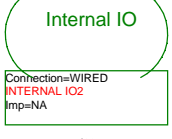
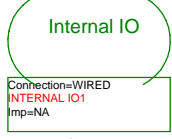
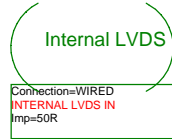
DEVICE=HD90_240F
 PARTS=STD
 PRG TYPE=HD90_240F
 HETERO=HD90_240F_IO1,HD90_240F_IO2,HD90_240F_IO3,HD90_240F_IO4
 HETERO_SYMNAME=HD90_240F_IO3

DAT_IN40	DGND	181
DAT_IN41	DGND	182
DAT_IN42	DGND	183
DAT_IN43	DGND	184
DAT_IN44	DGND	185
DAT_IN45	DGND	186
DAT_IN46	DGND	187
DAT_IN47	DGND	188
DAT_IN48	DGND	189
DAT_IN49	DGND	190
DAT_IN50	DGND	191
DAT_IN51	DGND	192
DAT_IN52	DGND	193
DAT_IN53	DGND	194
DAT_IN54	DGND	195
DAT_IN55	DGND	196
DAT_IN56	DGND	197
DAT_IN57	DGND	198
DAT_IN58	DGND	199
GTL+32	DGND	209
GTL+33	DGND	210
GTL+34	DGND	211
GTL+35	DGND	212
GTL+36	DGND	213
GTL+37	DGND	214
GTL+38	DGND	215
GTL+39	DGND	216
GTL+40	DGND	217
GTL+41	DGND	218
GTL+42	DGND	219
GTL+43	DGND	220
GTL+44	DGND	221
GTL+45	DGND	222
GTL+46	DGND	223
GTL+47	DGND	224

IO4

SYM

DEVICE=HD90_240F
 PARTS=STD
 PRG TYPE=HD90_240F
 HETERO=HD90_240F_IO1,HD90_240F_IO2,HD90_240F_IO3,HD90_240F_IO4
 HETERO_SYMNAME=HD90_240F_IO4



DGND	2	J2	1	LVDS IC IN8+
DGND	4	3	LVDS IC IN4-	
DGND	6	5	LVDS IC IN7-	
DGND	8	7	LVDS IC IN7+	
DGND	10	9	LVDS IC IN6+	
DGND	12	11	LVDS IC IN6-	
DGND	14	13	LVDS IC IN5-	
DGND	16	15	LVDS IC IN5+	
DGND	18	17	LVDS IC IN4-	
DGND	20	19	LVDS IC IN4+	
DGND	22	21	LVDS IC IN3-	
DGND	24	23	LVDS IC IN3+	
DGND	26	25	LVDS IC IN2-	
DGND	28	27	LVDS IC IN2+	
DGND	30	29	LVDS IC IN1-	
DGND	32	31	LVDS IC IN1+	
DGND	34	33	LVDS IC CLK IN-	
DGND	36	35	LVDS IC CLK IN+	

HEAD2X18_M

DGND	2	J21	2	DAT IN40
DGND	3	4	DAT IN41	
DGND	5	6	DAT IN42	
DGND	7	8	DAT IN43	
DGND	9	10	DAT IN44	
DGND	11	12	DAT IN45	
DGND	13	14	DAT IN46	
DGND	15	16	DAT IN47	
DGND	17	18	DAT IN48	
DGND	19	20	DAT IN49	
DGND	21	22	DAT IN50	
DGND	23	24	DAT IN51	
DGND	25	26	DAT IN52	
DGND	27	28	DAT IN53	
DGND	29	30	DAT IN54	
DGND	31	32	DAT IN55	
DGND	33	34	DAT IN56	
DGND	35	36	DAT IN57	
DGND	37	38	DAT IN58	
DGND	39	40	DAT IN59	
DGND	41	42	DAT IN60	

DIP2x21

DGND	3	J23	2	VDD
DGND	4	4	3.3V	
DGND	5	6	DAT_IN79	
DGND	7	8	DAT_IN78	
DGND	9	10	DAT_IN77	
DGND	11	12	DAT_IN76	
DGND	13	14	DAT_IN75	
DGND	15	16	DAT_IN74	
DGND	17	18	DAT_IN73	
DGND	19	20	DAT_IN72	
DGND	21	22	DAT_IN71	
DGND	23	24	DAT_IN70	
DGND	25	26	DAT_IN69	
DGND	27	28	DAT_IN68	
DGND	29	30	DAT_IN67	
DGND	31	32	DAT_IN66	
DGND	33	34	DAT_IN65	
DGND	35	36	DAT_IN64	
DGND	37	38	DAT_IN63	
DGND	39	40	DAT_IN62	
DGND	41	42	DAT_IN61	

DIP2x21

Only Internal Connections

DAT_OUT39	DGND	1
DAT_OUT38	DGND	2
DAT_OUT37	DGND	3
DAT_OUT36	DGND	4
DAT_OUT35	DGND	5
DAT_OUT34	DGND	6
DAT_OUT33	DGND	7
DAT_OUT32	DGND	8
DAT_OUT31	DGND	9
DAT_OUT30	DGND	10
DAT_OUT29	DGND	11
DAT_OUT28	DGND	12
DAT_OUT27	DGND	13
DAT_OUT26	DGND	14
DAT_OUT25	DGND	15
DAT_OUT24	DGND	16
DAT_OUT23	DGND	17
DAT_OUT22	DGND	18
DAT_OUT21	DGND	19
DAT_OUT20	DGND	20
DAT_OUT19	DGND	21
DAT_OUT18	DGND	22
DAT_OUT17	DGND	23
DAT_OUT16	DGND	24
DAT_OUT15	DGND	25
DAT_OUT14	DGND	26
DAT_OUT13	DGND	27
DAT_OUT12	DGND	28
DAT_OUT11	DGND	29
DAT_OUT10	DGND	30
DAT_OUT9	DGND	31
DAT_OUT8	DGND	32
DAT_OUT7	DGND	33
DAT_OUT6	DGND	34
DAT_OUT5	DGND	35
DAT_OUT4	DGND	36
DAT_OUT3	DGND	37
DAT_OUT2	DGND	38
DAT_OUT1	DGND	39
DAT_OUT0	DGND	40

DEVICE=HD90_240M
PARTS=1
PRG_TYPE=HD90_240M
HD90_240M_IO1,HD90_240M_IO2,HD90_240M_IO3,HD90_240M_IO4
HETERO_SYMNAME=HD90_240M_IO1

IO1

LVDS_B2B_OUT1+	DGND	61
LVDS_B2B_OUT1-	DGND	62
LVDS_B2B_OUT2+	DGND	63
LVDS_B2B_OUT2-	DGND	64
LVDS_B2B_OUT3+	DGND	65
LVDS_B2B_OUT3-	DGND	66
LVDS_B2B_OUT4+	DGND	67
LVDS_B2B_OUT4-	DGND	68
LVDS_B2B_OUT5+	DGND	69
LVDS_B2B_OUT5-	DGND	70
LVDS_B2B_OUT6+	DGND	71
LVDS_B2B_OUT6-	DGND	72
LVDS_B2B_OUT7+	DGND	73
LVDS_B2B_OUT7-	DGND	74
LVDS_B2B_OUT8+	DGND	75
LVDS_B2B_OUT8-	DGND	76
GTL+0	DGND	87
GTL+1	DGND	88
GTL+2	DGND	89
GTL+3	DGND	90
GTL+4	DGND	91
GTL+5	DGND	92
GTL+6	DGND	93
GTL+7	DGND	94
GTL+8	DGND	95
GTL+9	DGND	96
GTL+10	DGND	97
GTL+11	DGND	98
GTL+12	DGND	99
GTL+13	DGND	100
GTL+14	DGND	101
GTL+15	DGND	102
GTL+16	DGND	103
GTL+17	DGND	104

IO2

SYM

DEVICE=HD90_240M
PARTS=1
PRG_TYPE=HD90_240M
HD90_240M_IO1,HD90_240M_IO2,HD90_240M_IO3,HD90_240M_IO4
HETERO_SYMNAME=HD90_240M_IO2

GTL+18	DGND	121
GTL+19	DGND	122
GTL+20	DGND	123
GTL+21	DGND	124
GTL+22	DGND	125
GTL+23	DGND	126
GTL+24	DGND	127
GTL+25	DGND	128
GTL+26	DGND	129
GTL+27	DGND	130
GTL+28	DGND	131
GTL+29	DGND	132
GTL+30	DGND	133
GTL+31	DGND	134
DAT_OUT59	DGND	143
DAT_OUT60	DGND	144
DAT_OUT61	DGND	145
DAT_OUT62	DGND	146
DAT_OUT63	DGND	147
DAT_OUT64	DGND	148
DAT_OUT65	DGND	149
DAT_OUT66	DGND	150
DAT_OUT67	DGND	151
DAT_OUT68	DGND	152
DAT_OUT69	DGND	153
DAT_OUT70	DGND	154
DAT_OUT71	DGND	155
DAT_OUT72	DGND	156
DAT_OUT73	DGND	157
DAT_OUT74	DGND	158
DAT_OUT75	DGND	159
DAT_OUT76	DGND	160
NC		175
NC		176
NC		177
3 3V		178
3 3V		179
3 3V		180

IO3

SYM

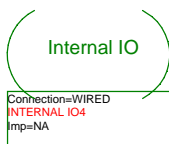
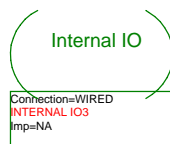
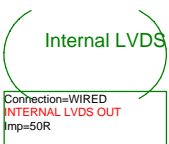
DEVICE=HD90_240M
PARTS=1
PRG_TYPE=HD90_240M
HD90_240M_IO1,HD90_240M_IO2,HD90_240M_IO3,HD90_240M_IO4
HETERO_SYMNAME=HD90_240M_IO3

DAT_OUT40	DGND	181
DAT_OUT41	DGND	182
DAT_OUT42	DGND	183
DAT_OUT43	DGND	184
DAT_OUT44	DGND	185
DAT_OUT45	DGND	186
DAT_OUT46	DGND	187
DAT_OUT47	DGND	188
DAT_OUT48	DGND	189
DAT_OUT49	DGND	190
DAT_OUT50	DGND	191
DAT_OUT51	DGND	192
DAT_OUT52	DGND	193
DAT_OUT53	DGND	194
DAT_OUT54	DGND	195
DAT_OUT55	DGND	196
DAT_OUT56	DGND	197
DAT_OUT57	DGND	198
DAT_OUT58	DGND	199
GTL+32	DGND	200
GTL+33	DGND	201
GTL+34	DGND	202
GTL+35	DGND	203
GTL+36	DGND	204
GTL+37	DGND	205
GTL+38	DGND	206
GTL+39	DGND	207
GTL+40	DGND	208
GTL+41	DGND	209
GTL+42	DGND	210
GTL+43	DGND	211
GTL+44	DGND	212
GTL+45	DGND	213
GTL+46	DGND	214
GTL+47	DGND	215

IO4

SYM

DEVICE=HD90_240M
PARTS=1
PRG_TYPE=HD90_240M
HD90_240M_IO1,HD90_240M_IO2,HD90_240M_IO3,HD90_240M_IO4
HETERO_SYMNAME=HD90_240M_IO4



DGND	1	2	LVDS IC CLK OUT+
DGND	3	4	LVDS IC CLK OUT-
DGND	5	6	LVDS IC OUT1+
DGND	7	8	LVDS IC OUT1-
DGND	9	10	LVDS IC OUT2+
DGND	11	12	LVDS IC OUT2-
DGND	13	14	LVDS IC OUT3+
DGND	15	16	LVDS IC OUT3-
DGND	17	18	LVDS IC OUT4+
DGND	19	20	LVDS IC OUT4-
DGND	21	22	LVDS IC OUT5+
DGND	23	24	LVDS IC OUT5-
DGND	25	26	LVDS IC OUT6+
DGND	27	28	LVDS IC OUT6-
DGND	29	30	LVDS IC OUT7+
DGND	31	32	LVDS IC OUT7-
DGND	33	34	LVDS IC OUT8+
DGND	35	36	LVDS IC OUT8-

HEADZK18_M

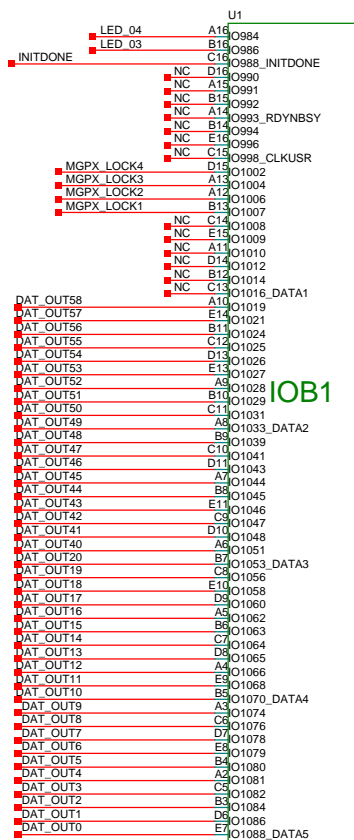
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DGND	3	4	DAT OUT1
DGND	5	6	DAT OUT2
DGND	7	8	DAT OUT3
DGND	9	10	DAT OUT4
DGND	11	12	DAT OUT5
DGND	13	14	DAT OUT6
DGND	15	16	DAT OUT7
DGND	17	18	DAT OUT8
DGND	19	20	DAT OUT9
DGND	21	22	DAT OUT10
DGND	23	24	DAT OUT11
DGND	25	26	DAT OUT12
DGND	27	28	DAT OUT13
DGND	29	30	DAT OUT14
DGND	31	32	DAT OUT15
DGND	33	34	DAT OUT16
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DGND	37	38	DAT OUT18
DGND	39	40	DAT OUT19
DGND	41	42	DAT OUT20

DIP2x21

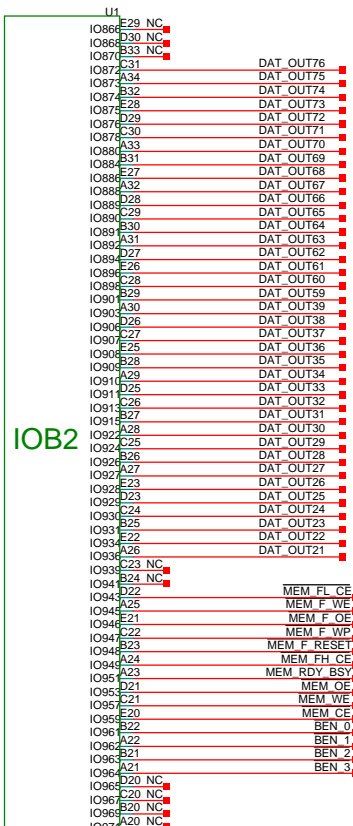
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DGND	3	4	DAT OUT22
DGND	5	6	DAT OUT23
DGND	7	8	DAT OUT24
DGND	9	10	DAT OUT25
DGND	11	12	DAT OUT26
DGND	13	14	DAT OUT27
DGND	15	16	DAT OUT28
DGND	17	18	DAT OUT29
DGND	19	20	DAT OUT30
DGND	21	22	DAT OUT31
DGND	23	24	DAT OUT32
DGND	25	26	DAT OUT33
DGND	27	28	DAT OUT34
DGND	29	30	DAT OUT35
DGND	31	32	DAT OUT36
DGND	33	34	DAT OUT37
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DGND	39	40	3 3V
DGND	41	42	VDD

DIP2x21

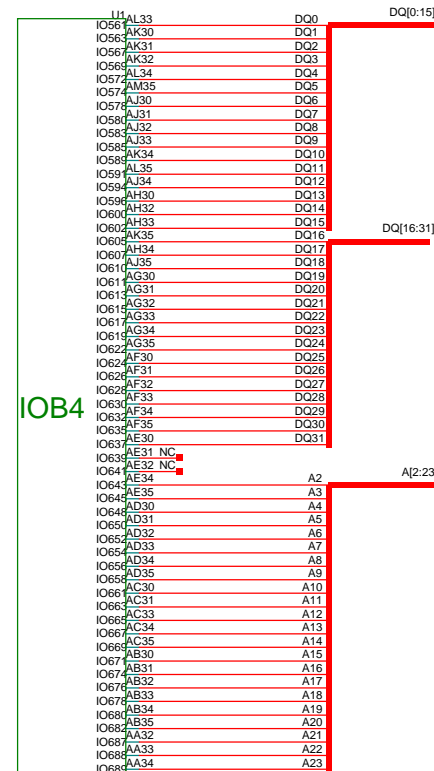
El Camino GmbH
Title
megAPEX Connector Out
Document Name
MGPX_V01
Author
FH
Date
9-17-2001_16:00
Sheet
3



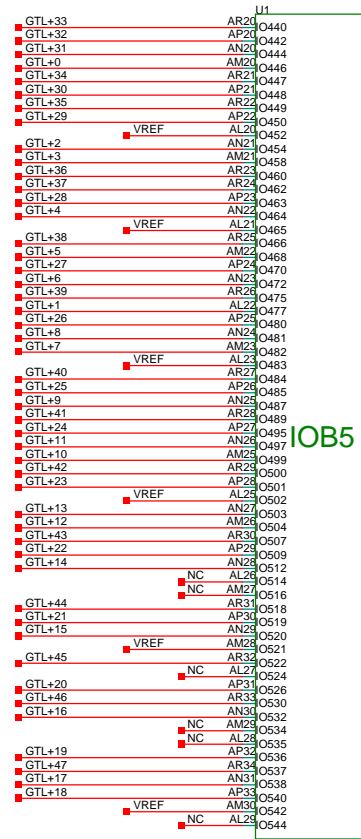
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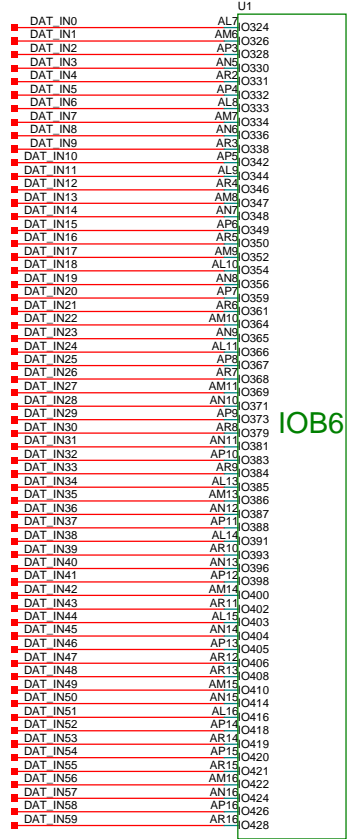
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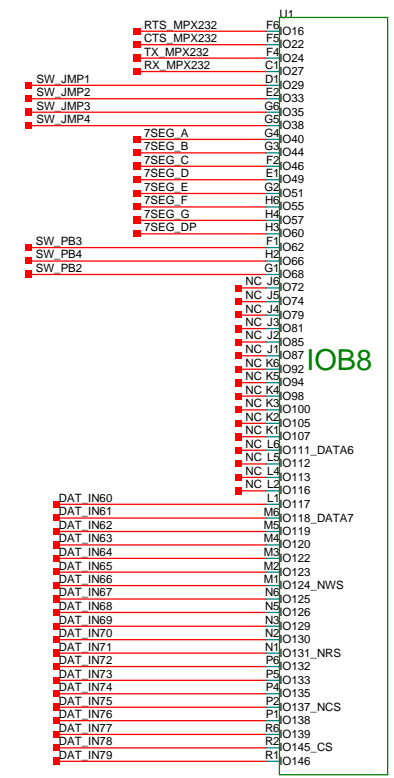
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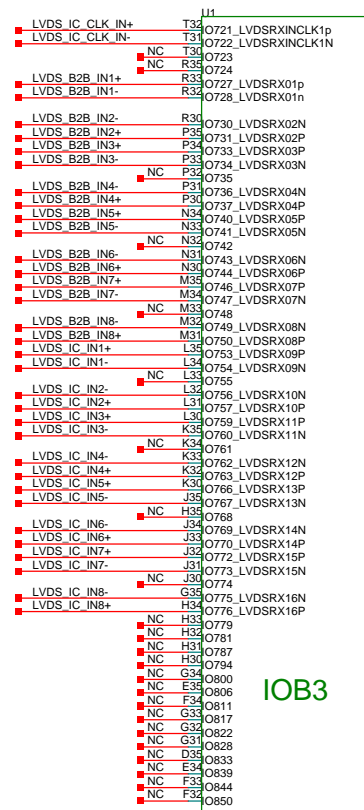
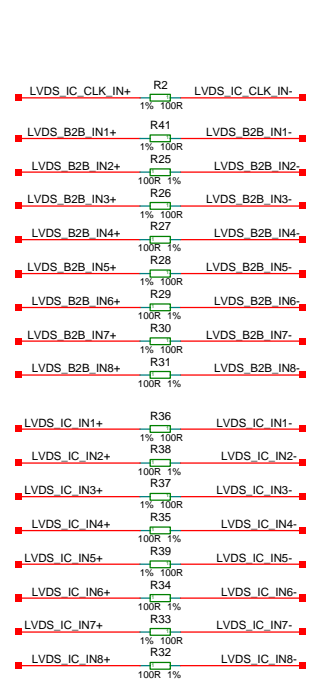
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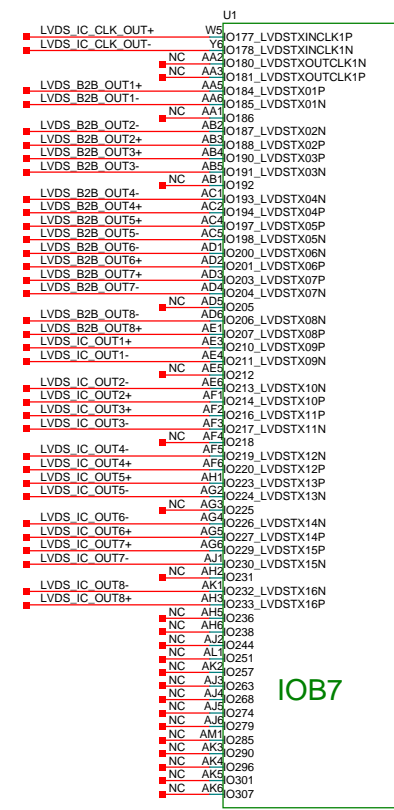
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 PARTS=1
 LEVEL=STD
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 PARTS=1
 LEVEL=STD
 HETERO_SYMMNAME=20K15IOB8



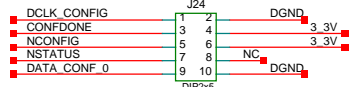
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 HETERO_SYMMNAME=20K15IOB3



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 PARTS=10
 HETERO_SYMMNAME=20K15IOB7

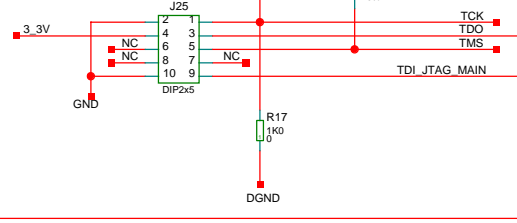
Master Blaster or Byteblaster

Conhction=WIRED
BLASTER
Imp=NA



JTAG

Conhction=WIRED
JTAG
Imp=NA



JTAG

U1
AN15 TCK_5_438
AM15 TMS_5_439
D15 TRST_1_973
W15 TDO_1_982

DEVICE=EP20K1500
PARTS=1
LEVEL=STD
PRG_TYPE=BGA652
HETERO_SYMNAME=20K15JTAG

default closed

Conhction=JUMPER
NA
Imp=NA

default closed

Conhction=JUMPER
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CONFIG

U15

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PARTS=1

RY_BY# 24 NC

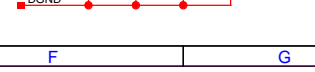
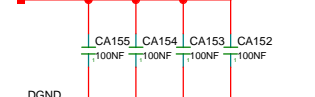
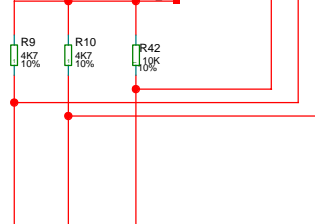
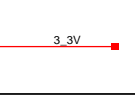
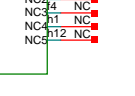
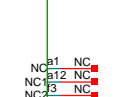
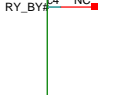
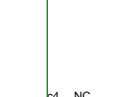
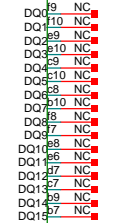
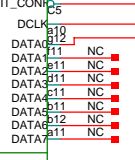
NC 11 NC
NC 12 NC
NC 13 NC
NC 14 NC
NC 15 NC
NC 16 NC

h11 VDD6
h12 VDD5
h13 VDD4
h14 VDD3
h15 VDD2
h16 VDD1
h17 VDD0
h18 VCCW
h19 VCCB
h20 VCC8
h21 VCC4
h22 VCC3
h23 VCC2
h24 VCC1
h25 VCC

h1 VDD6
h2 VDD5
h3 VDD4
h4 VDD3
h5 VDD2
h6 VDD1
h7 VDD0
h8 VCCW
h9 VCCB
h10 VCC8
h11 VCC4
h12 VCC3
h13 VCC2
h14 VCC1
h15 VCC

h1 VDD6
h2 VDD5
h3 VDD4
h4 VDD3
h5 VDD2
h6 VDD1
h7 VDD0
h8 VCCW
h9 VCCB
h10 VCC8
h11 VCC4
h12 VCC3
h13 VCC2
h14 VCC1
h15 VCC

h1 VDD6
h2 VDD5
h3 VDD4
h4 VDD3
h5 VDD2
h6 VDD1
h7 VDD0
h8 VCCW
h9 VCCB
h10 VCC8
h11 VCC4
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Title
megAPEX CONF, JTAG

Document Name MGPX_V01 Author FH

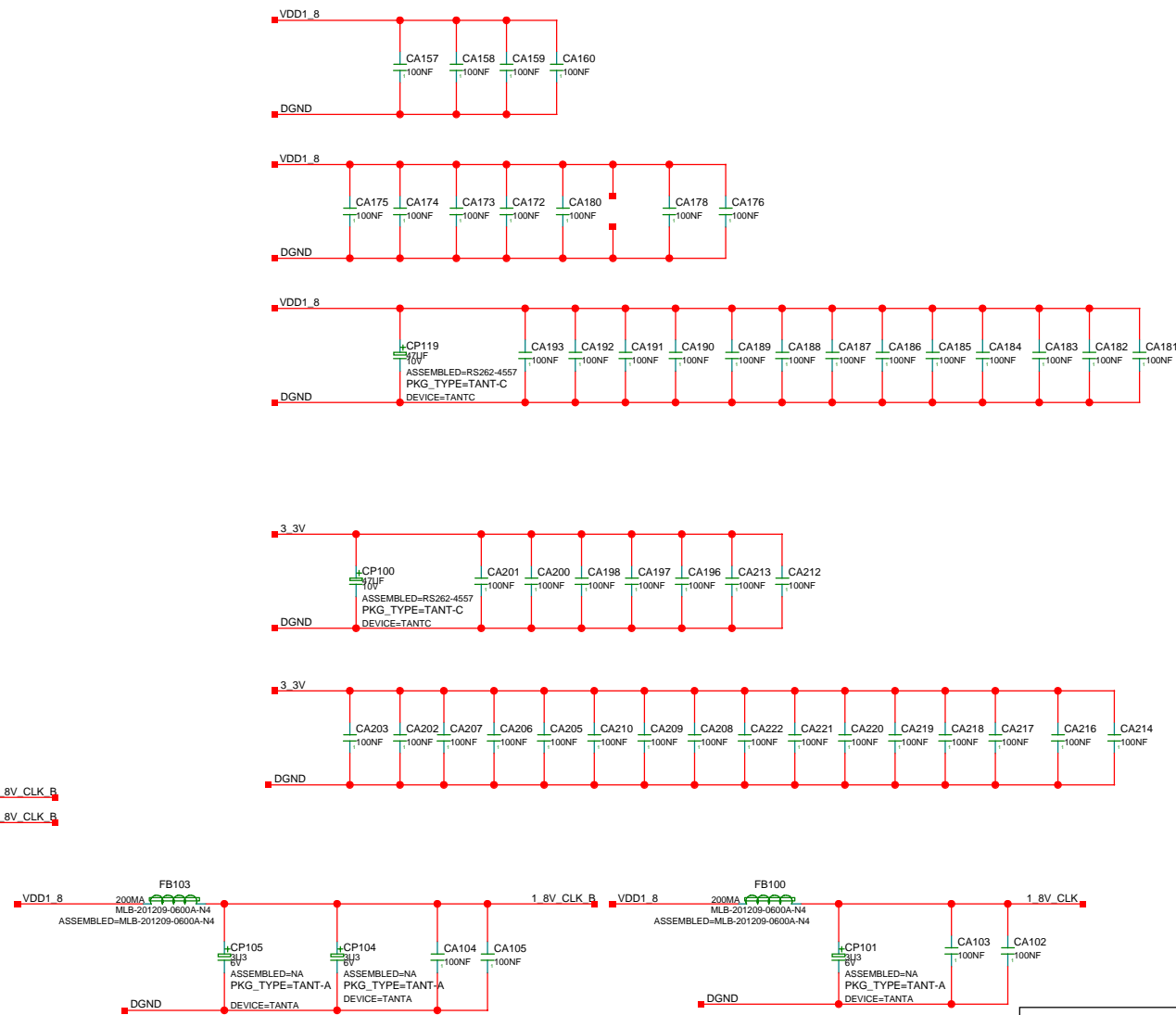
Date 9-17-2001_16:00 Sheet 7

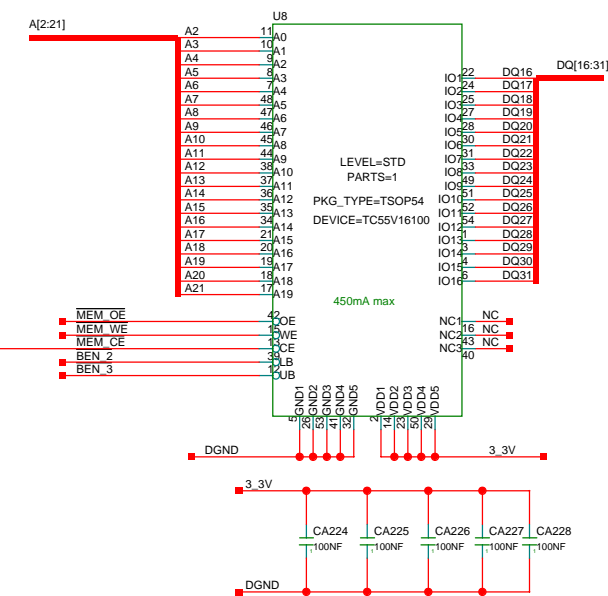
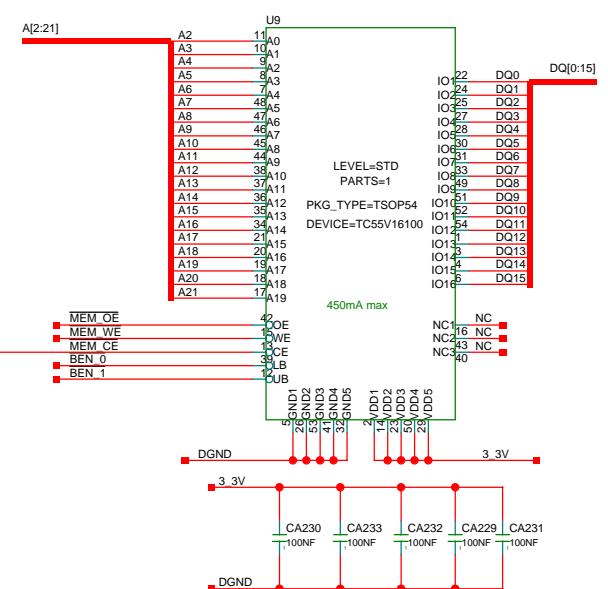
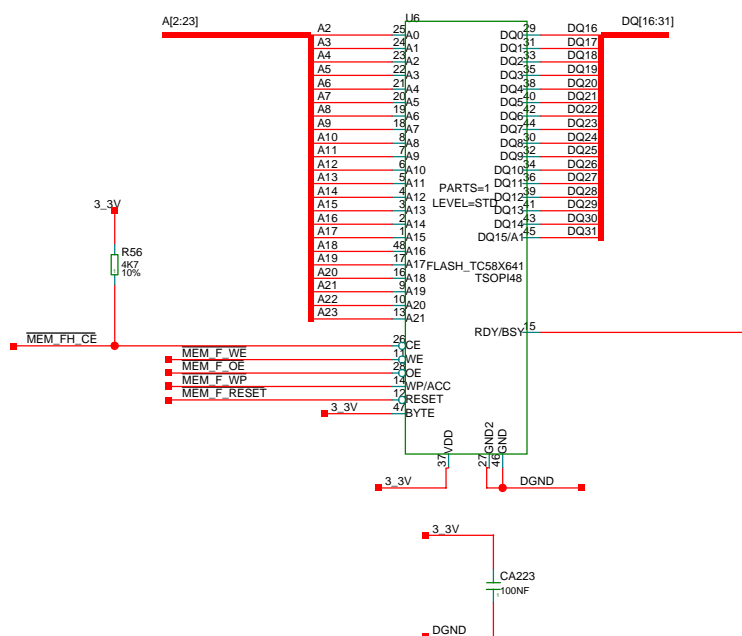
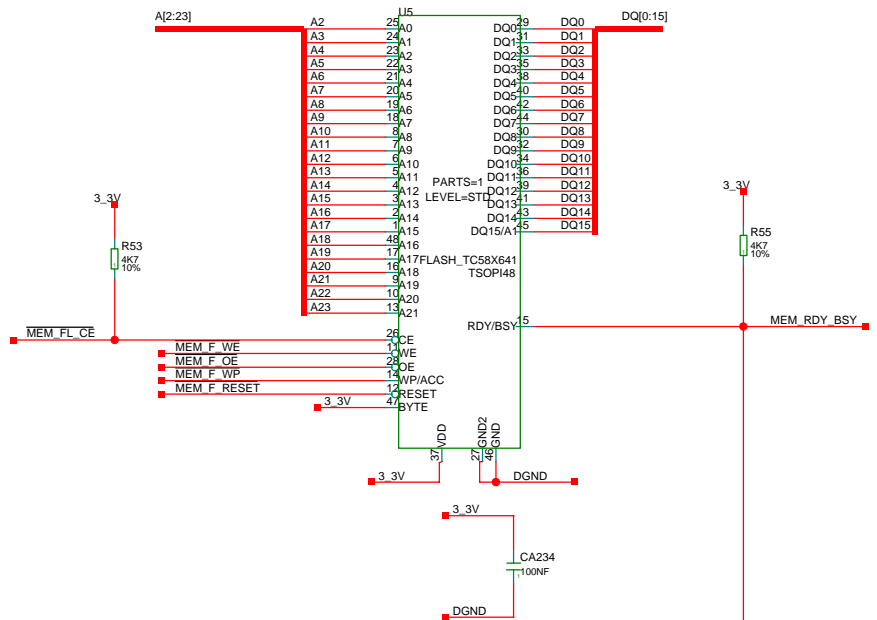
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DGND	A18	GND_A18	VCCL_A19	VDD1_8
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DGND	AK18	GND_AK18	VCCL_AA4	VDD1_8
DGND	AL18	GND_AL18	VCCL_AC3	VDD1_8
DGND	AL30	GND_AL30	VCCL_AC32	VDD1_8
DGND	AL6	GND_AL6	VCCL_AE2	VDD1_8
DGND	AM18	GND_AM18	VCCL_AE33	VDD1_8
DGND	AM2	GND_AM2	VCCL_AG1	VDD1_8
DGND	AM3	GND_AM3	VCCL_AH3	VDD1_8
DGND	AM31	GND_AM31	VCCL_AH35	VDD1_8
DGND	AM32	GND_AM32	VCCL_AH4	VDD1_8
DGND	AM33	GND_AM33	VCCL_AK3	VDD1_8
DGND	AM34	GND_AM34	VCCL_AL12	VDD1_8
DGND	AM4	GND_AM4	VCCL_AL24	VDD1_8
DGND	AN18	GND_AN18	VCCL_AM12	VDD1_8
DGND	AN2	GND_AN2	VCCL_AR17	VDD1_8
DGND	AN3	GND_AN3	VCCL_AR19	VDD1_8
DGND	AN34	GND_AN34	VCCL_D12	VDD1_8
DGND	AN35	GND_AN35	VCCL_D24	VDD1_8
DGND	AP1	GND_AP1	VCCL_E12	VDD1_8
DGND	AP18	GND_AP18	VCCL_E24	VDD1_8
DGND	AP2	GND_AP2	VCCL_F3	VDD1_8
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DGND	AP34	GND_AP34	VCCL_G30	VDD1_8
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DGND	AR18	GND_AR18	VCCL_H5	VDD1_8
DGND	AR35	GND_AR35	VCCL_H5	VDD1_8
DGND	B1	GND_B1	VCCL_K3	VDD1_8
DGND	B18	GND_B18	VCCL_L3	VDD1_8
DGND	B2	GND_B2	VCCL_M30	VDD1_8
DGND	B3	GND_B3	VCCL_M30	VDD1_8
DGND	B35	GND_B35	VCCL_N35	VDD1_8
DGND	C18	GND_C18	VCCL_N4	VDD1_8
DGND	C2	GND_C2	VCCL_R34	VDD1_8
DGND	C3	GND_C3	VCCL_R5	VDD1_8
DGND	C33	GND_C33	VCCL_U34	VDD1_8
DGND	C34	GND_C34	VCCL_U3	VDD1_8
DGND	C35	GND_C35	VCCL_W31	VDD1_8
DGND	D17	GND_D17	VIO1_C4	3.3V
DGND	D18	GND_D18	VIO1_D5	3.3V
DGND	D2	GND_D2	VIO1_E17	3.3V
DGND	D3	GND_D3	VIO2_E19	3.3V
DGND	D32	GND_D32	VIO2_D31	3.3V
DGND	D33	GND_D33	VIO2_D31	3.3V
DGND	D34	GND_D34	VIO2_C32	3.3V
DGND	D4	GND_D4	VIO3_F30	3.3V
DGND	E18	GND_E18	VIO3_F31	3.3V
DGND	E30	GND_E30	VIO3_F3	3.3V
DGND	E31	GND_E31	VIO3_U30	3.3V
DGND	E32	GND_E32	VIO4_W30	3.3V
DGND	E33	GND_E33	VIO4_AL31	3.3V
DGND	E5	GND_E5	VIO4_AL32	3.3V
DGND	E6	GND_E6	VIO4_AL32	3.3V
DGND	F18	GND_F18	VIO5_AN33	3.3V
DGND	V1	GND_V1	VIO5_AN33	3.3V
DGND	V2	GND_V2	VIO5_AL19	3.3V
DGND	V3	GND_V3	VIO6_AL17	3.3V
DGND	V30	GND_V30	VIO6_AM5	3.3V
DGND	V31	GND_V31	VIO6_AN4	3.3V
DGND	V32	GND_V32	VIO7_AL3	3.3V
DGND	V33	GND_V33	VIO7_AL4	3.3V
DGND	V34	GND_V34	VIO7_W6	3.3V
DGND	V4	GND_V4	VIO8_U6	3.3V
DGND	V5	GND_V5	VIO8_E3	3.3V
DGND	V6	GND_V6	VIO8_E4	3.3V
DGND	Y30	GND_CLK1	VCC_CLK	1.8V_CLK_B
DGND	W2	GND_CLK2	VCC_CLK	1.8V_CLK_B
DGND	W3	GND_CLK3	VCC_CLK	1.8V_CLK_B
DGND	V35	GND_CLK4	VCC_CLK	1.8V_CLK_B
DGND	R3	GND_CLK5	VCC_CLK	1.8V_CLK_B
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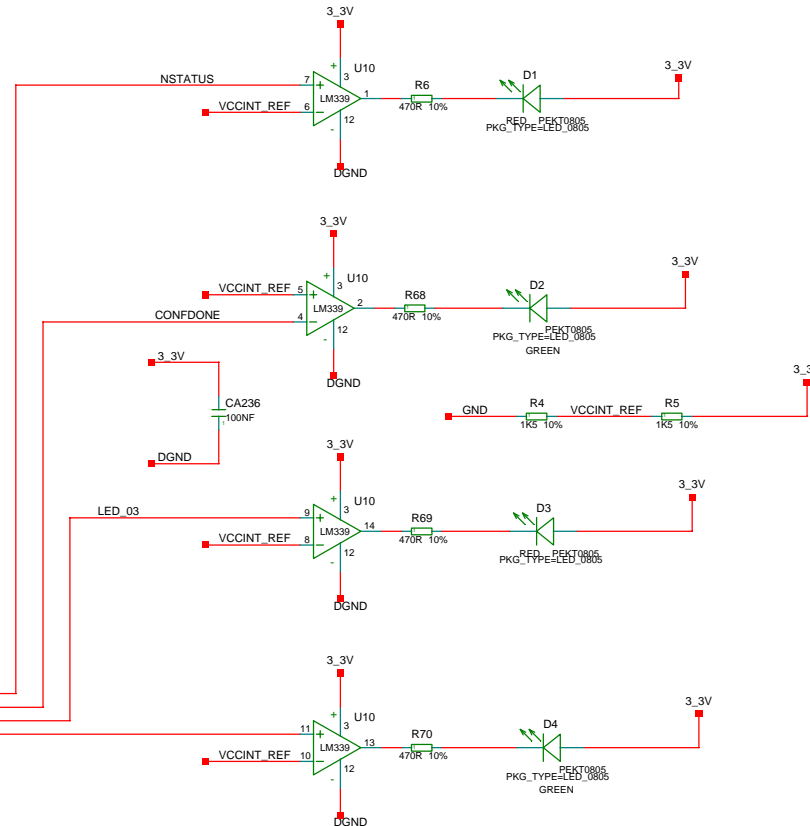
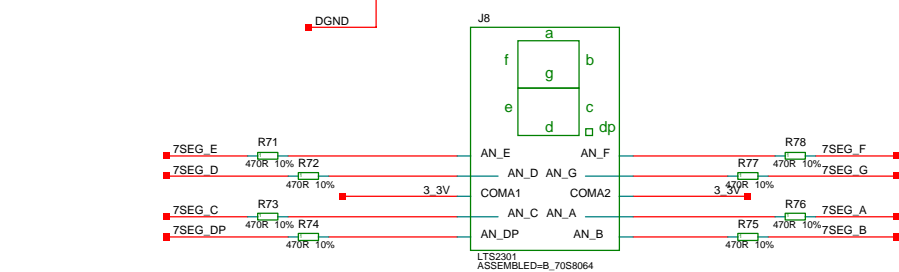
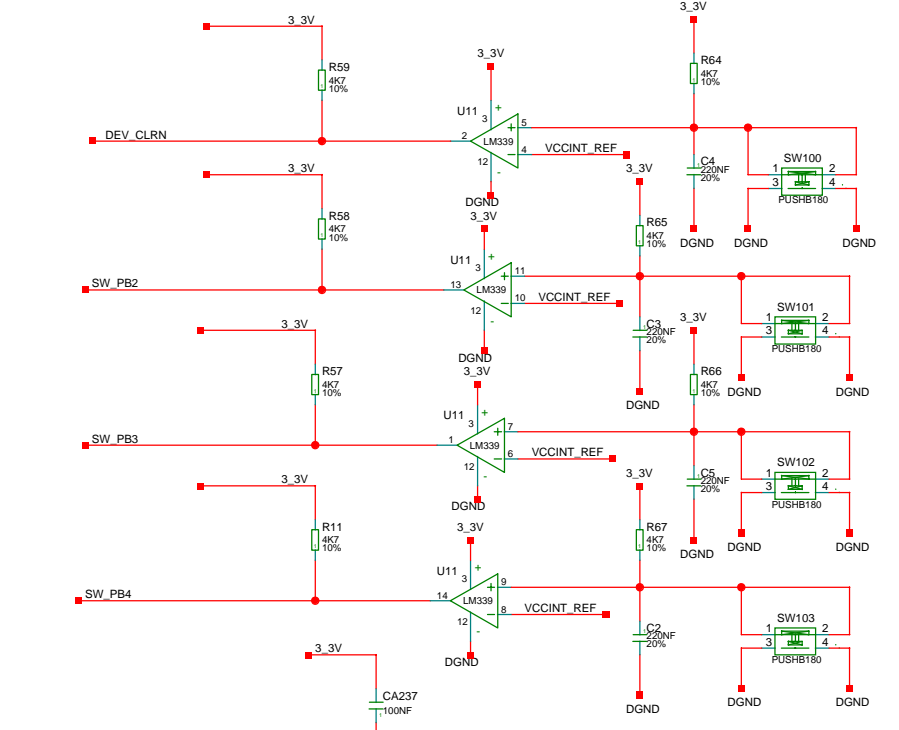
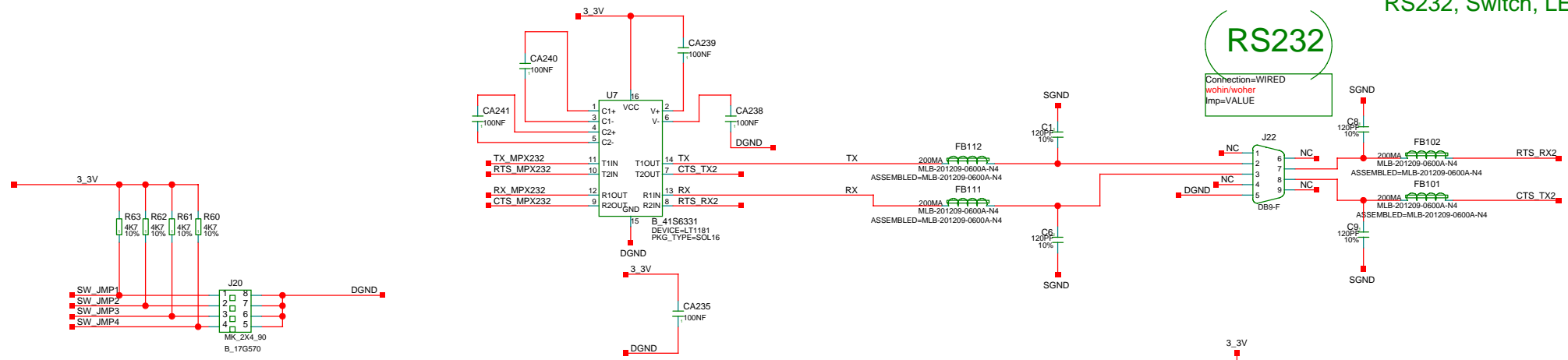
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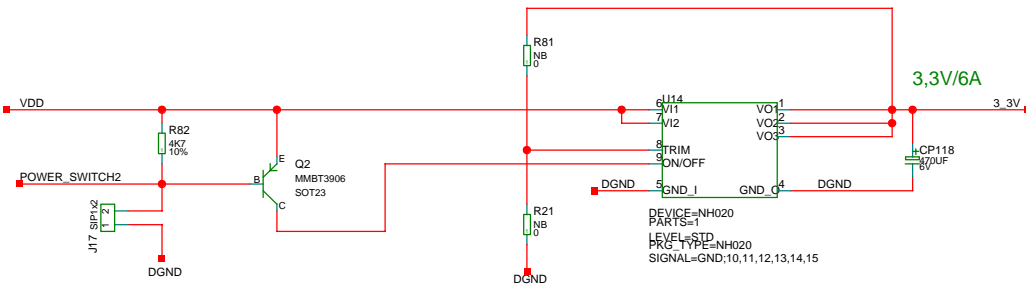
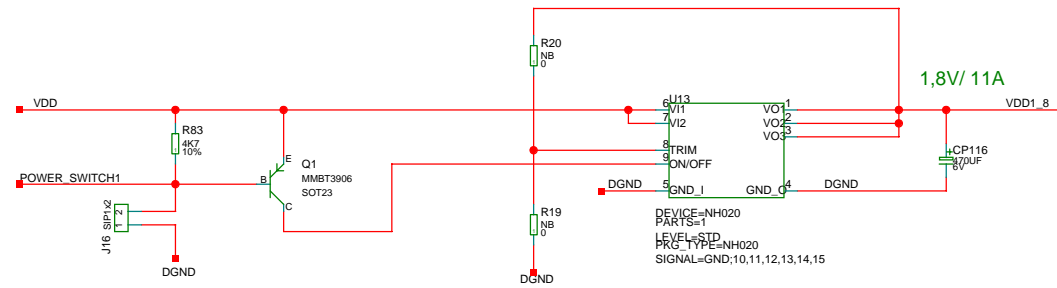
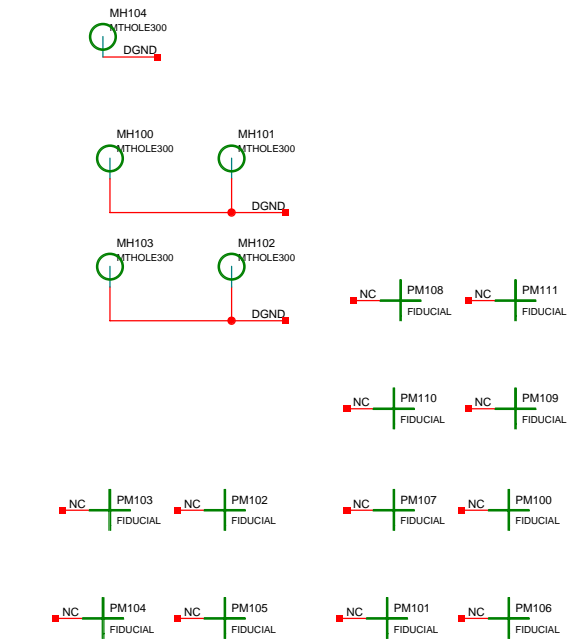
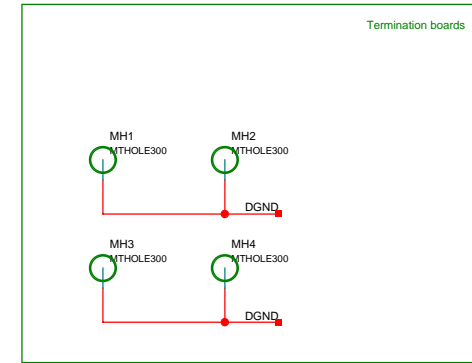
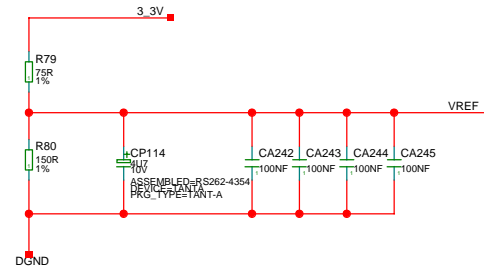
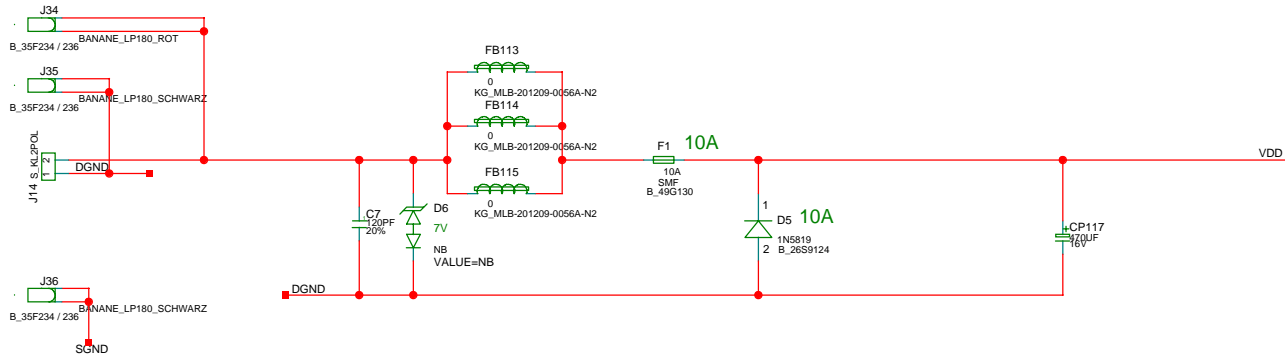
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 PARTS
 LEVEL=STD
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 HETERO_SYMNAME=20K15PWR





RS232
Connetion=WIRED
Wohin/woher
Imp=VALUE





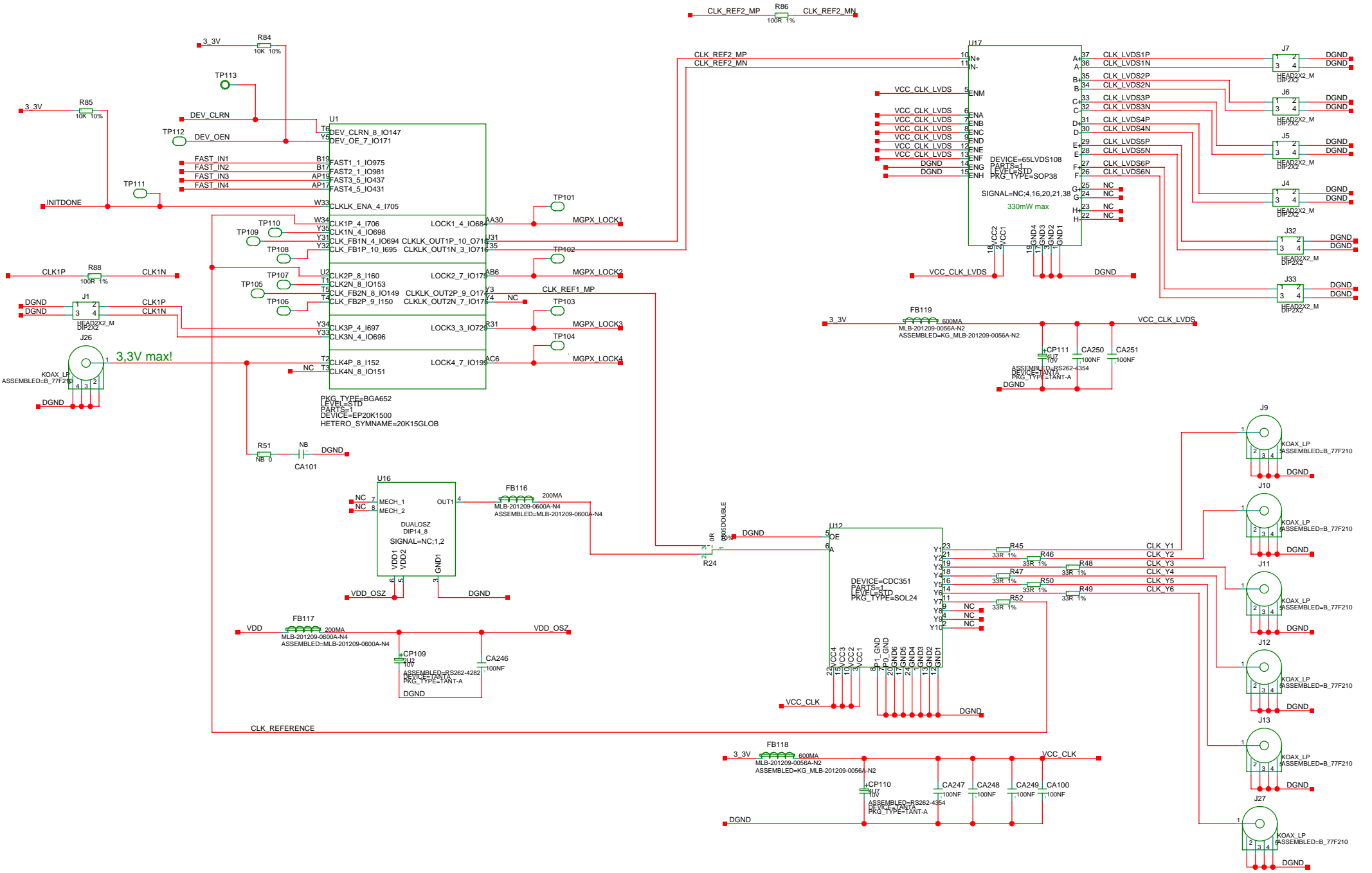
El Camino GmbH

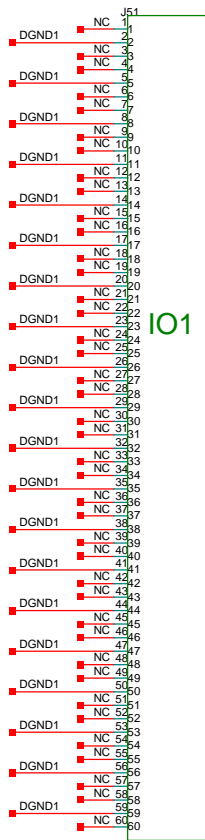
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Document Name MGPX_V01 Author FH

Date 9-17-2001_16:00 Sheet 11

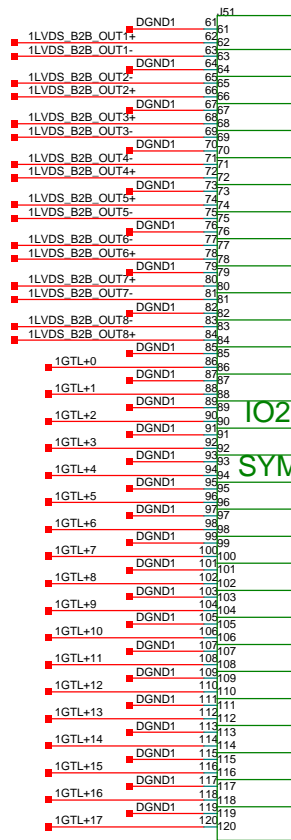
CLK Tree





IO1

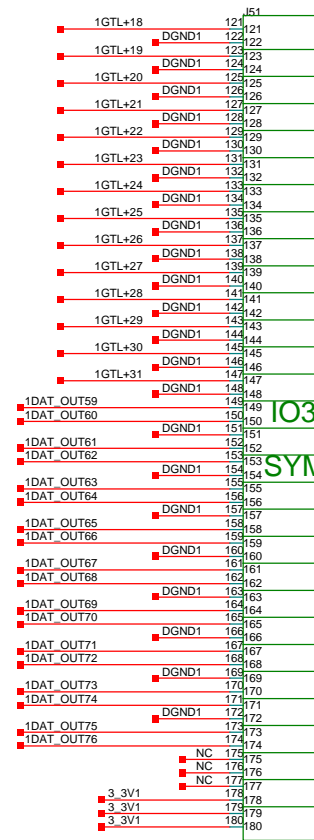
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IO2

SYM

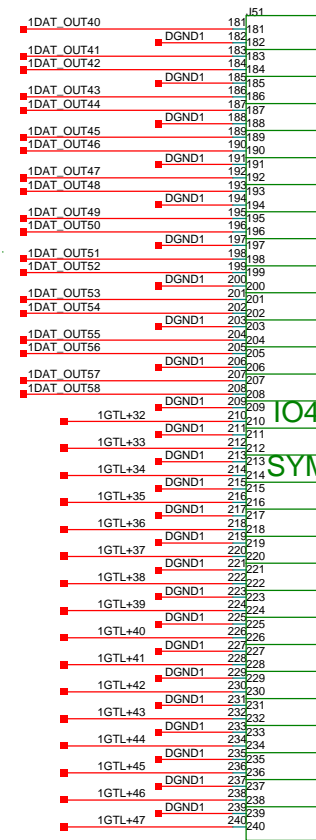
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HETERO_SYMMNAME=HD90_240F_IO2



IO3

SYM

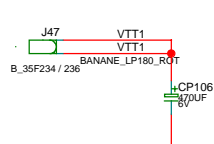
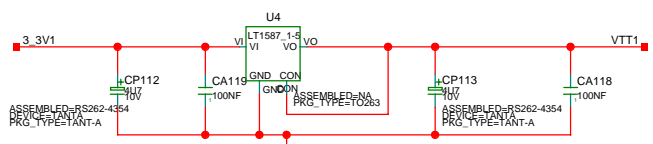
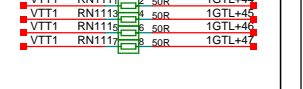
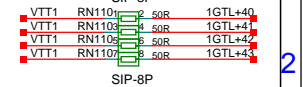
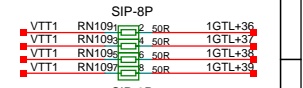
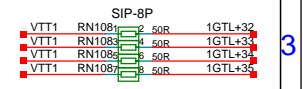
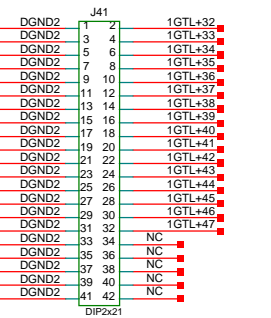
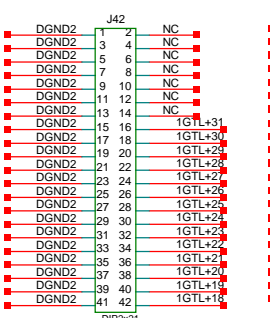
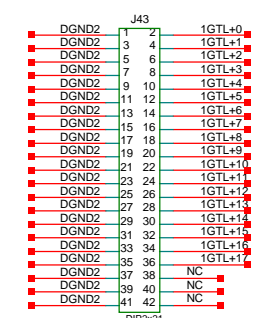
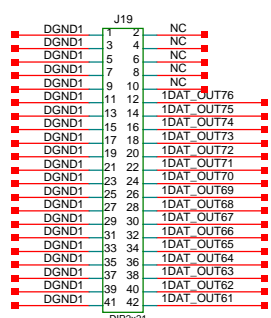
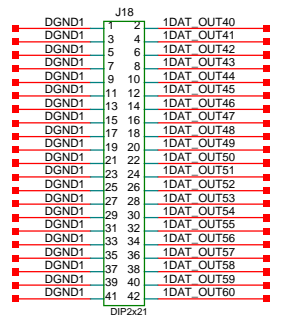
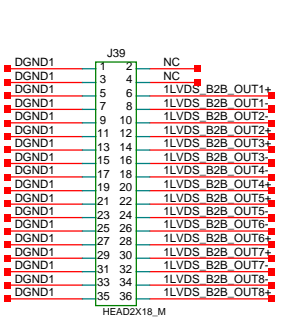
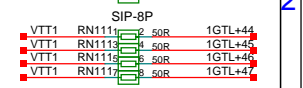
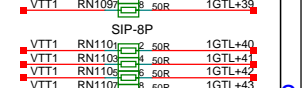
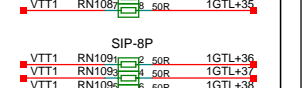
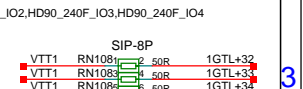
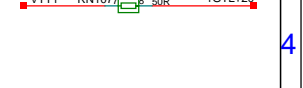
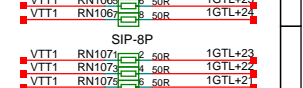
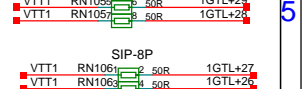
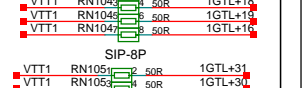
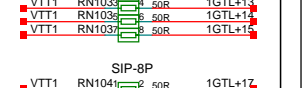
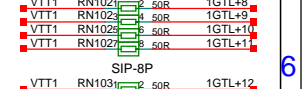
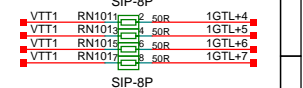
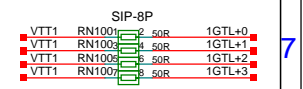
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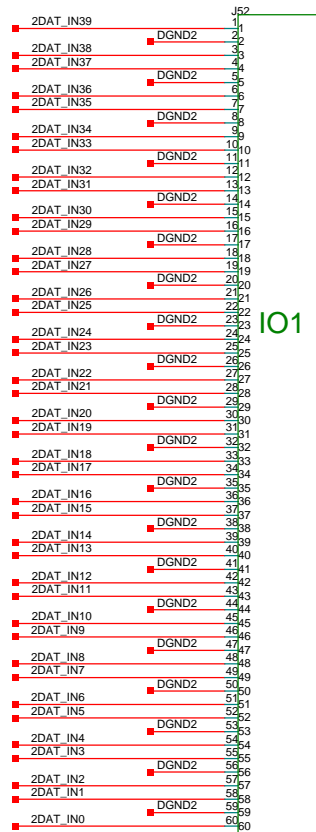
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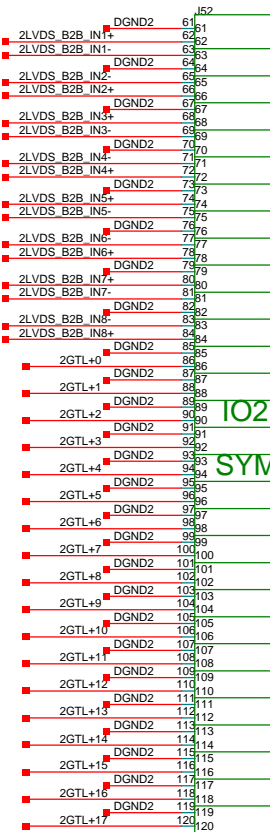
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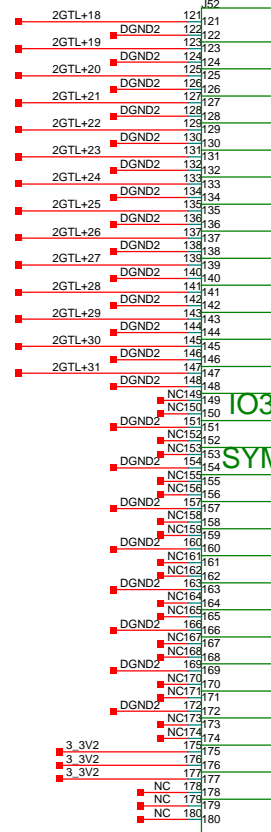
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megAPEX Connector Termination Out
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Date 7-27-2001 10:14



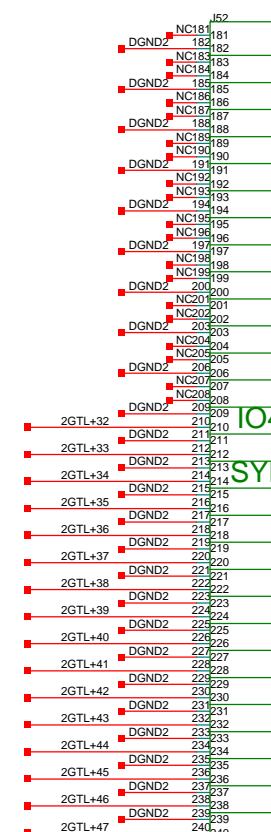
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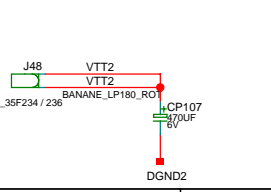
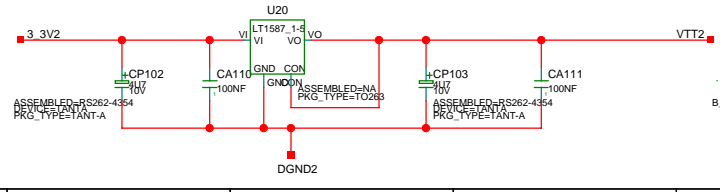
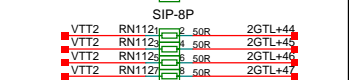
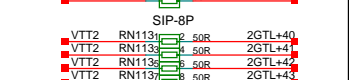
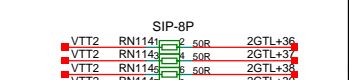
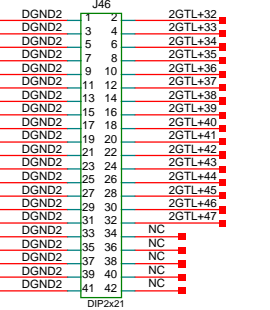
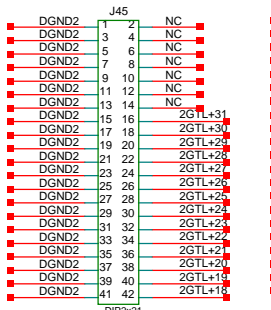
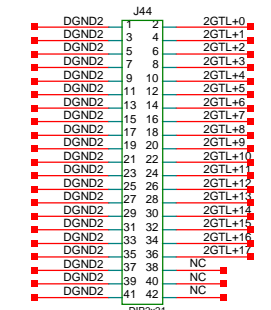
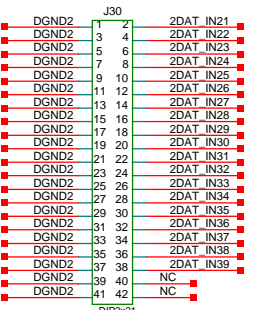
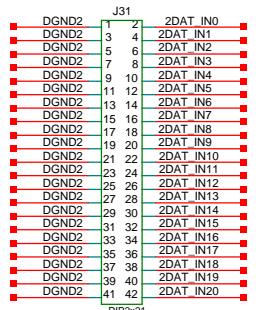
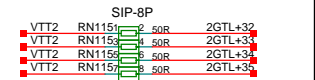
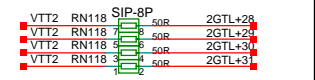
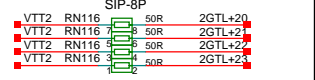
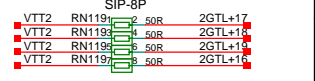
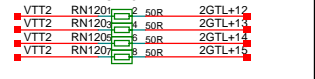
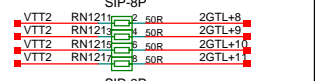
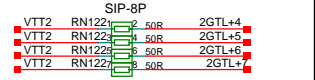
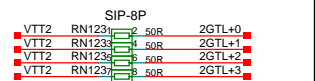
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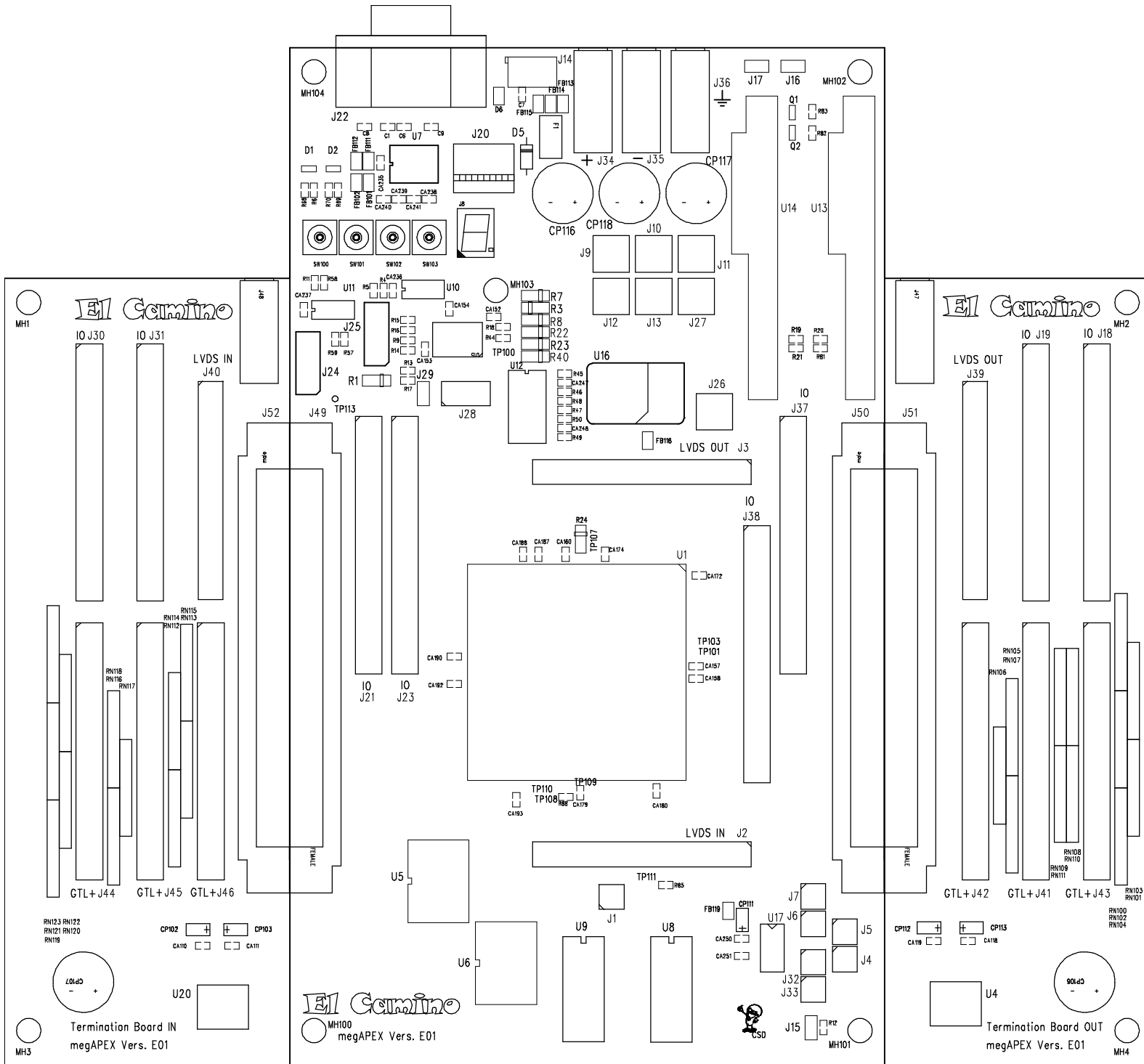
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El Camino GmbH
 Title: megAPEX Connector Termination In
 Document Name: MGPX_V01
 Date: 7-27-2001 10:14
 Author: FH
 Sheet: 14



Top

