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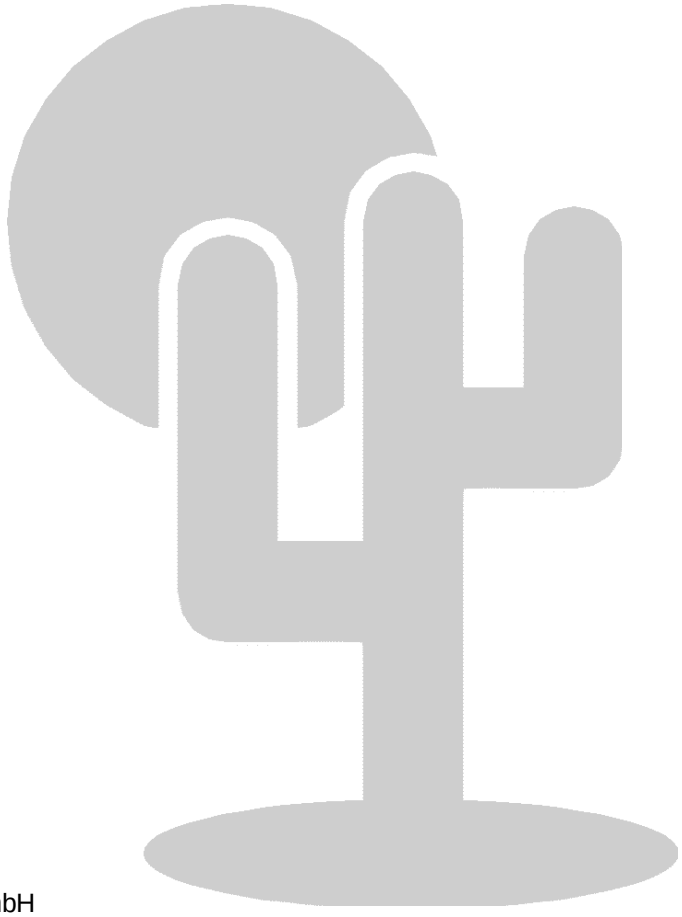
DIGILAB 20Kx240 MANUAL

APEX™ 20K Prototyping System



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Chapter
1

Digilab 20Kx240 – Preface

General Description

The DIGILAB 20Kx240 is intended for prototyping based on Altera's APEX 20K devices. It supports all APEX 20K devices in the QFP240 package (including E-family).

DIGILAB 20Kx240 Features:

- Comes with your choice of APEX 20K device in (R)QFP 240 package (APEX 20K or APEX 20KE)
- 17-146 User I/Os (depends on which on-board functions are used)
- 4-Layer PCB in Europe-Standard format
- 1-2 Configuration Flash EPROMs EPC2 on board
- Bi-colour status LED for STATUS, CONFDONE
- Debounced reboot/reset push buttons
- JTAG-Input/-Output for Cascading multiple Modules
- Insertion Slots for either one sub-module in Europe-Standard format or two individual sub-modules in half the size
- Three individual operating voltages (VCC-IO, VCC-INT, VCC-AUX) @ 5V, 3.3V, 2.5V or 1.8V
- Two individual independent SRAM Banks with 512kx16 each fast SRAM
- Optional socket for 28DIL or 32DIL (EE/E)PROM
- Driver and connector for USB (USB-A or USB-B)
- Optional quartz oscillator, rectangular or squared outline
- PLL support
- 4-digit, multiplexed 7- segment display
- Four bicolour LEDs
- Four pushbuttons
- Connector for interfacing with DSP (e.g. SHARC-DSP-Eazy-Kit) SPORT- or LINK-Interface as an option

Warning:
This is a class A device. This device may cause radio interference in the living area.
The user may be required to carry out and be responsible for appropriate measures.

Chapter
2

Board Description

Disable Functions and Reserve Inputs

In order to avoid contention on the board make sure you follow the following guidelines. Disabling on-board functions also allows the use of associated signals for your own, custom applications.

1. Disable all functions that are not required

Function	To Disable	Signal Name	APEX 20K Pin
Memory Bank 0 (left), LSB	drive high	CSU8X	115
Memory Bank 0 (left), MSB	drive high	CSU7X	80
Memory Bank 1 (right), LSB	drive high	CSU10X	237
Memory Bank 2 (right), MSB	drive high	CSU9X	223
(EE)PROM (optional)	drive high	CS_ROMX	239
Serial EEPROM, U5	drive high	SEEP_CSX	184
USB-A, U17	pull JP11		
	pull JP12		
	pull JP13		
USB-B, U16	pull JP14		
	pull JP15		
	pull JP16		

2. Implement Inputs in your design for those functions that can't be disabled

Function	To Disable	Signal Name	APEX 20K Pin
Push Button S1	reserve input	KEY_S1	61
Push Button S2	reserve input	KEY_S2	50
Push Button S3	reserve input	KEY_S3	63
Push Button S4	reserve input	KEY_S4	57

3. Some pins that are VCC or GND pins in larger APEX 20K devices are general purpose user I/Os in smaller devices. These pins are connected to VCC or GND on the DIGILAB 20Kx240 in order to support the largest device in QFP 240. Such pins are listed in the table on the next page and need to be reserved as unused inputs in your design.

Always Reserve these Pins as Unused Inputs

Function in larger devices	APEX 20K Pin	EP20K100	EP20K200	EP20K60E	EP20K100E	EP20K160E	EP20K200E	EP20K300E
VCC_INT	5	X		TBD	X	X		
	14	X			X			
	39	X			X	X		
	52	X			X			
	73	X	X		X	X	X	
	107	X	X		X	X	X	
	127	X			X			
	140	X			X	X		
	168	X			X			
	176	X			X	X		
	193	X	X		X	X	X	
	227	X	X		X	X	X	
VCC_PLL	22	X	X		X	X	X	
	25	X	X		X	X	X	
	37	X	X		X	X	X	
	142	X	X					
	159	X	X					
GND_INT	6	X			X	X		
	15	X			X			
	38	X			X	X		
	51	X			X			
	72	X	X		X	X	X	
	106	X	X		X	X	X	
	128	X			X			
	167	X			X			
	175	X			X	X		
	194	X	X		X	X	X	
	228	X	X		X	X	X	
GND_PLL	21	X	X		X	X	X	
	24	X	X		X	X	X	
	36	X	X		X	X	X	
	141	X	X					
	158	X	X					

X pin is driven on the board, reserve as unused input in your design!

Voltage Regulators and Power Supply

There are three voltage regulators on the board (VCC_INT, VCC_IO, VCC_AUX). Depending on the device they may be set to different voltages.

VCC_INT is the internal voltage of the APEX device. This voltage is fixed and not user-selectable. VCC_INT is generated by the regulator U11.

	APEX 20K	APEX 20KE
VCC_INT (fixed)	2.5 V	1.8 V

VCC_IO is the supply-voltage for the APEX-IOs and can also be used to supply some on board devices such as the Memory, USB etc. VCC_IO is generated by U12. You can select between two different fixed values just by connecting or disconnecting JP5.

	JP5	
	open (default)	closed
VCC_IO	3.3 V	2.5 V

VCC_AUX is an additional supply voltage that you may use in your application. It is generated by U13. You can select between two different fixed values by connecting JP6. As a default setting none of the on-board devices use VCC_AUX. You need to consider whether 5V tolerance is exists for the APEX 20K inputs when using 5V VCC_AUX.

	JP6	
	open	closed (default)
VCC_AUX	5.0 V	3.3 V

The following table shows the limits (minimum and maximum) for the input voltage of the board. Please consider that an input voltage much above the maximum value will cause excessive heat on the board.

	V_{IN} MIN	V_{IN} MAX
$V_{CC\ AUX}$ = 5 V	7.5 V	12.0 V
$V_{CC\ AUX}$ = 3.3 V	5.8 V	12.0 V

Maximum/Minimum Input Voltage

The required current will depend largely on your design and the clock frequency.

Configuration

There are four different ways to configure the APEX device:

1. Configuration via JTAG-Interface
2. From the EPC2
3. Parallel mode
4. Serial mode from an external processor

Description of the JTAG-Chain:
To setup the JTAG-Chain properly you need to consider the following details. The JTAG-chain starts at P6. Normally, a Byte-Blaster, Master-Blaster or the output of another board is connected to this plug.

You have the possibility to feed the JTAG chain to your own devices on the daughter board 1. Therefore the JTAG-signals feeds to P1B where you can insert your own JTAG-capable devices in the chain.
If you don't use this feature or no daughter board is used at all you need to connect the signal TDI with TDI_EPC. Setting the jumper JP1 will do this for you (default setting).

The JTAG-chain is then connected to the first (U2) and second (U3) EPC2 device. Depending on the type of APEX-device there are one or two EPC2 on your board. If only one device is required it must be installed on U2 and the jumper JP3 must be installed.

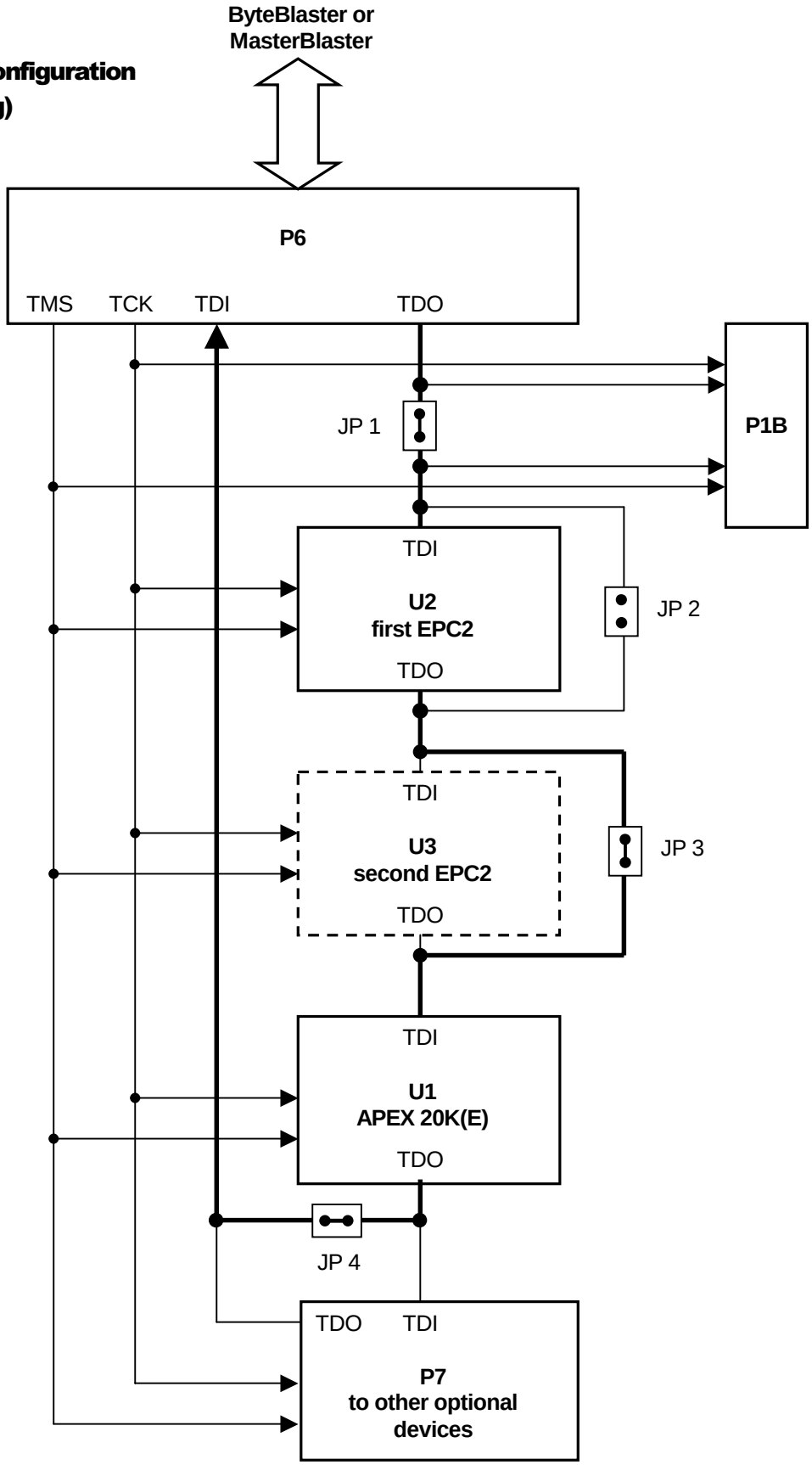
Next, the JTAG chain feeds the APEX-device and goes on to P7. It allows to connect additional boards to your JTAG chain. If you don't need this feature, JP4 must be installed (default).

The JTAG-chain in the programmer window needs to be setup in the same order as it is physically implemented on the board:

(Devices on daughter board, optional) => first EPC2 (U2) => second EPC2 (U3, if required) => APEX device => (additional devices on another board connected to P7, optional).

The picture on the next page shows a block diagram of the JTAG chain

JTAG Chain Configuration (default setting)



When you have finished the setup you should check the chain with your configuration software (Quartus or MAX+plus II). Now you are ready to either configure the APEX and/or program the EPC2(s) via the JTAG-Interface.

Once you have programmed the EPC2s the APEX-device configures itself every time the board is powered up. You can force a reconfiguration either with a JTAG-command which is executed by U2 or U3, via S6 (reconfigure button), by downloading a new configuration or re-programming the EPC2s (U2,U3).

LED5 is connected to the CONF_DONE and NSTATUS outputs of the APEX 20K device and gives you the status of the configuration.

		LED 5
Configuration Error	NSTATUS = low	red
Configuration Successful	CONF_DONE = high	green

If you want to use the parallel-mode configuration you can easily access all necessary signals via connector P2A. For parallel configuration, BR1 and BR2 (MSEL0 and MSEL1 inputs) must be changed properly. Per default they are set to serial configuration.

To implement a serial configuration performed form an alternative device (e.g. a microprocessor) instead of the EPC2s, both EPC2s (U2, U3) need to be removed. You can then use P8 to connect your own signals (DCLK, DATA0, CONF_DONE, NSTATUS, NCONFIG).

Global Reset

There is a global reset switch (S5) which feeds the global reset input (DEV_CLRn) of the APEX device. This switch is already debounced to avoid problems. If you want to use the global reset feature it must be enabled in the Device Settings in the Compiler.

Memory

There are two independent banks of memory (memory bank0/left, memory bank1/right), each up to 512K by 16. Independent means that there are separate address-, data- and control-lines for each of the banks. It enables the APEX device to access both memories in one clock-cycle with independent addresses and data. This is useful for e.g. FFT-applications. Nevertheless, connecting the addresses internally enables also building a single wide (32 Bit) memory for other applications.

If specific applications require only one memory bank or no external memory at all, the according CSx-lines should be pulled to a logic high level. The memory is then inactive and you can use the IO-ports of the APEX device for other purposes

The supply-voltage of both memories can be chosen independently via BR7 (left memory) and BR5 (right memory). Normally they should be connected to VCC_IO (default setting).

The right memory bank shares it's data lines with the data lines required for configuration in parallel mode (except D0). This is useful because the lower data lines of the microprocessor have to be connected to this IOs when you use this configuration mode.

In addition, the right memory bank has a socket for a standard ROM, PROM, (E)EPROM or FLASH device in a 28/32 pin DIL standard JEDEC package. Some pins (RL1, RL31) which have different function depending on the type of device being used, are fed to the APEX separately. The remaining addresses and data lines are shared with the right RAM bank.

The supply voltage can be selected separately via BR11 for this device. BR14 selects between 28 or 32 pin device. You need to take care about the voltage compatibility between the device and the according APEX IO-pins.

		Chip Select	drive to	APEX 20K Pin
Memory Bank 0 (left)	LSB	CSU8X	high	115
	MSB	CSU7X	high	80
Memory Bank 1 (right)	LSB	CSU10X	high	237
	MSB	CSU9X	high	223
(EE)PROM (optional)	LSB	CS_ROMX	high	239

Disable Memory

Serial EEPROM

There is serial EEPROM (93C46A) on the board. This device can be used to store some user defined, nonvolatile data. For a description and the protocol (serial read and write) please refer to the 93C46A datasheet e.g. from Atmel.

If you don't use this device just make sure to pull the signal SEEP_CSx to a logic high level. The other signals connected to the device can then be used as APEX 20K user-IOs.

		Chip Select	drive to	APEX 20K Pin
Serial EEPROM	U5	SEEP_CSX	high	184

Disable Serial EEPROM

USB

The DIGILAB 20Kx240 has two USB-drivers (PDIUSBP11A, U17/U18) and two spaces for USB-connectors. Since there are two different types of USB-connectors (Type A and Type B) they are not soldered to the board. Two connectors of each type come with your board and you can install the one you need by yourself or leave it unpopulated.

If you don't need the USB functionality you may disconnect JP11, JP12, JP13 and JP14, JP15, JP16 accordingly. By doing so, you can use all APEX 20K IO-pins associated with the according USB-drivers as regular user-IOs.

BR15 and BR16 select the speed (high or low) for the drivers. Depending on the kind of application you want to implement (Host or Device, High Speed or Low Speed) you need to populate BR17, BR18, BR19 and BR20 with either 1,5Kohm or 15Kohm resistors to GND or VCC. For details please refer to the USB-driver data sheet.

P5 and USB_B (U16) share IO-pins. Therefore only one of this function can be active at a time. The other one must be disabled.

ADSP-SPORT Interface

P5 can be used as high speed interface for connecting different other devices. Originally, it was designed to connect to the SPORT of an ADSP-SHARC Board. Nevertheless, it can also be used in other similar applications where a flat cable must be used because of it's defined impedance. On this connector a signal line is always surrounded by GND-lines.

An optional termination network (RN07) can be added.

P5 and USB_B (U16) share IO-pins. Therefore only one of these functions can be active at a time. The other one must be disabled.

Display and Switches

There is a 4-digit 7-segment multiplexed display on the board. A display driver macrofunction can be found on the web (http://www.elca.de).

Furthermore, there are 4 LEDs each capable of displaying two independent colors (red/green) and 4 push buttons. Please keep in mind that these buttons are not de-bounced. An example of a de-bouncing circuitry can also be found on the web-site.

If you don't need this functionality you can just disconnect the supply for these devices (BR13 for the Display, BR12 for the LEDs).

Multi Voltage Support

Two APEX 20K IO-Groups (Group 4 and Group 8) support the Altera MultiVolt feature. Care must be taken what else is driven by these ports (e.g. the display etc).

To enable multi voltage support BR25 and/or BR26 can be removed and the IO groups may be connected to a different power source.

Module Connectors and Daughter Boards

All relevant signals of the APEX device are accessible via 4 connectors, two on each side of the board (P1, P2, P3, P4).

Each connector itself consists of two parts. One is a 2 by 25 connector with a shell. This part allows to plug in a flat-wire connector or daughter board. In addition, there is another 25 pin connector (single line) which contains some auxiliary signals. Many pins of this connector are not populated which allows you to route your own signals to these pins.

You can plug in daughter boards with your specific circuitry. One of these daughter boards (with prototyping area) comes with your DIGILAB 20Kx240 board.

Two small or one large board can be connected.

P2 contains all signals that are needed for parallel configuration and the lower 8 address- and 8 data lines for the right memory block,

P4 contains the rest of the address- and data-lines of the right memory bank.

P1 contains parts of the left memory bank signals and the display/button control signals, P3 the rest of the left memory-bank signals.

96-Pin-Edge Connector (Optional)

There is additional board space for an optional 96/64-pin connector. By default no signals of the board are routed to this connector. It may be useful if you need to place the board into a 19" rack with a back plane connector.

It's only possible to use this connector while none of the USB-connectors (J1, J2) are populated and P5 does not conflict with it (that means no 90° connector for this one is used).

Clock Generation and PLL Support

There is a quartz-oscillator on board (default 48MHz) which can drive CLK1 and/or CLK3. Instead of the quartz-oscillator the master clock can be fed via J3 (optional). In case of using J3 the oscillator must be removed. All clock-signals on the board have a defined impedance of 50 ohm (stripeline). Optionally, the clocks can be terminated close to the clock pin of the APEX device (R9/C56 for CLK3, R10/C57 for CLK2, R11/C58 for CLK1, R12/C59 for CLK0).

	Resistor	Capacitor
CLK 0	R 12	C 59
CLK 1	R 11	C 58
CLK 2	R 10	C 57
CLK 3	R 9	C 56

Optional Clock Termination

CLK0 and CLK2 can be fed either by P2B (pins 52, 53) or by JP9, JP10. Unused clock pins must be tied to a fixed level (GND or VCCIO). This can be done by setting the jumpers JP9 and/or JP10, JP7, JP8.

There are up to 4 PLLs available, depending on the device installed.

The power supply for the PLLs is critical (affects jitter), therefore the PLL supply is decoupled in two groups (upper and lower PLLs) via a L/C combination. In case of special requirements the connection between VCCINT and VCCPLL can be disconnected by removing L1/L2. VCCPLL can then be applied from a different, special supply (e.g. special filter etc.).

When using the clock output (CLKOUT1/0) from the internal PLL and the feedback path (CLKFBIN1/0), it is necessary to close this feedback loop. It can either be done by inserting your own logic (e.g. an external clock driver feeding the rest of your logic) or, if not available by setting a jumper between CLKOUT1/0 and CLKFBIN1/0.

There is also one pin per PLL (Lockout0/1/2/3) indicating the lock-state of the according PLL.

Jumpers

Jumper	Description	open	closed
JP 1	JTAG-Chain to daughter board 1	Daughter board present	■ Daughter board not present
JP 2	JTAG-Chain, no U2 (EPC2)	■ First EPC2 present	First EPC2 not present
JP 3	JTAG-Chain, no U3 (second EPC2)	Second EPC2 present	■ Second EPC2 not present
JP 4	JTAG-Chain, connect to next board	JTAG chain continues on next board	■ JTAG chain doesn't continue on next board
JP 5	VCC-IO voltage	■ VCC-IO = 3.3 V	VCC-IO = 2.5 V
JP 6	VCC-AUX voltage	VCC-AUX = 5.0 V	■ VCC-AUX = 3.3 V
JP 7	Clock 1 Select	■ A-X CLK Input	B-X GND
JP 8	Clock 3 Select	A-X CLK Input	■ B-X GND
JP 9	Clock 0 Select	CLK Input	■ GND
JP 10	Clock 2 Select	CLK Input	■ GND
JP 11	USB-Driver A (U17) VP	■ N.C.	VP connected to APEX 20K
JP 12	USB-Driver A (U17) RCV	■ N.C.	RCV connected to APEX 20K
JP 13	USB-Driver A (U17) VM	■ N.C.	VM connected to APEX 20K
JP 14	USB-Driver B (U18) VP	■ N.C.	VP connected to APEX 20K
JP 15	USB-Driver B (U18) RCV	■ N.C.	RCV connected to APEX 20K
JP 16	USB-Driver B (U18) VM	■ N.C.	VP connected to APEX 20K

■ default setting

Bridges

Bridge	Description	A-X or closed	B-X
BR 1	U1, MSEL 0	■ GND	VCC_IO
BR 2	U1, MSEL 1	■ GND	VCC_IO
BR 3	EPC2, VPP select	■ GND	VCC_EPC (see BR 6)
BR 4	EPC2, VCC select	■ GND	VCC_EPC (see BR 6)
BR 5	Memory Bank 1, right, VCC select	■ VCC_IO	VCC_AUX
BR 6	VCC_EPC select	■ VCC_IO	VCC_AUX
BR 7	Memory Bank 0, left, VCC select	■ VCC_IO	VCC_AUX
BR 8	VCC_OSC select	■ VCC_IO	VCC_AUX
BR 9	VCC_USB select	■ VCC_IO	VCC_AUX
BR 10	VCC_BY select (serial EPROM)	■ VCC_IO	VCC_AUX
BR 11	VCC_ROM select	■ VCC_IO	VCC_AUX
BR 12	VCC_LED select	■ VCC_IO	VCC_AUX
BR 13	VCC_SEG select	■ VCC_IO	VCC_AUX
BR 14	ROM (U6), address A17	■ RA17 (APEX I/O)	VCC_ROM
BR 15	USB-B (U16), speed select	GND	VCC_USB
BR 16	USB-A (U17), speed select	GND	VCC_USB
BR 17	USB-A (U16), function select (D+)	GND	VCC_USB
BR 18	USB-A (U16), function select (D-)	GND	VCC_USB
BR 19	USB-B (U17), function select (D+)	GND	VCC_USB
BR 20	USB-B (U17), function select (D-)	GND	VCC_USB
BR 21	JTAG out (P7), VCC	VCC_BY	
BR 22	Serial Configuration (P8), VCC	VCC_BY	
BR 23	USB-A (U16), mode	■ GND	
BR 24	USB-B (U17), mode	■ GND	
BR 25	U1, MultiVolt IO group 4	■ VCC_IO	
BR 26	U1, MultiVolt IO group 8	■ VCC_IO	
BR 27	U1, NCE input	■ GND	

■ default setting

User Connector Counting

P1A P2A

2	4	6	8	10	12				46	48	50
□ 1	3	5	7	9	11				45	47	49

P1B P2B

51	52	53	54	55	56				73	74	75

□ Square pad on bottom side marks pin 1

P3B P4B

51	52	53	54	55	56				73	74	75

P3A P4A

2	4	6	8	10	12				46	48	50
□ 1	3	5	7	9	11				45	47	49

□ Square pad on bottom side marks pin 1

User Connector Pinout P1

P1A				P1B	
1	GND	2		51	GND
3		4		52	
5	CS U7X	6	LA 0	53	
7	LA 1	8	LA 2	54	TCK
9	LA 3	10	LA 17	55	TMS
11	LOENX	12	LA 7	56	TDI
13	LA 6	14	LA 5	57	TDI_EPC
15	LA 4	16	LD 9	58	
17	GND	18		59	GND
19	LD 8	20	LD 14	60	VCC_IO
21	LD 15	22	SEG_C	61	
23	SEG_F	24	SEG_D	62	
25	SEG_A	26	SEG_E	63	
27	SEG_B	28	SEG_DP	64	
29	SEG_G	30	KEY_S4	65	
31	DIG 4	32	LD4_GN	66	
33	GND	34		67	GND
35	LD3_GN	36	LD4_RT	68	VCC_AUX
37	DIG 3	38	LD3_RT	69	
39	KEY_S3	40	KEY_S2	70	
41	KEY_S1	42	DIG 2	71	
43	LD2_GN	44	LD2_RT	72	
45	LD1_GN	46	LD1_RT	73	
47	DIG 1	48		74	
49	GND	50		75	GND

User Connector Pinout P2

P2A				P2B	
1	GND	2	CLKOUT 0	51	GND
3		4	CLKFBIN 0	52	CLK 2
5	FAST 1	6	FAST 0	53	CLK 0
7	IO143DOE	8	IO156DCL	54	
9	IO164NWS	10	IO161NRS	55	
11	IO160NCS	12	IO157CS	56	
13	IO205RDY	14	CDAT	57	
15	LOCKOUT 2	16	IO206IDO	58	
17	GND	18		59	GND
19		20	LOCKOUT 0	60	VCC_IO
21		22		61	
23	A_VMO	24		62	
25	RA 3	26	RA 0	63	
27	RA 1	28	RA 2	64	
29	RD 0	30	RA 4	65	
31	RD 2	32	RD 1	66	
33	GND	34		67	GND
35	RD 6	36	RD 3	68	VCC_AUX
37	RD 4	38	RD 5	69	
39	A_VP	40	RD 7	70	
41	RA 5	42	RA 6	71	
43	A_VPO	44	RA 7	72	
45	A_SUSP	46		73	
47	A_VM	48		74	
49	GND	50		75	GND

User Connector Pinout P3

P3A				P3B	
1	GND	2		51	GND
3		4		52	
5	LWENX	6	LA 8	53	
7	LA 16	8	LA 9	54	
9	LA 15	10	LA 10	55	
11	LA 13	12	LA 14	56	
13	LA 18	14	CSUBX	57	
15	LD 1	16	LD 0	58	
17	GND	18		59	GND
19	LD 2	20	LD 3	60	VCC_IO
21	LD 5	22	LA 11	61	
23	LA 12	24	LD 4	62	RECONFSW
25	LD 10	26	LD 6	63	
27		28		64	
29	LD 13	30	LD 11	65	GCLRSW
31		32	LD 12	66	
33	GND	34		67	GND
35		36	LD 7	68	VCC_AUX
37	IO 134	38	IO 166 (Pin 66)	69	
39	IO 125	40	IO 131	70	
41	IO 133	42	IO 126	71	
43		44	IO 124	72	
45	SEEP_SK	46	IO 130	73	
47	LOCKOUT 3	48	SEEP_DI	74	
49	GND	50		75	GND

User Connector Pinout P4

P4A				P4B	
1	GND	2	CLKOUT 1	51	GND
3		4	CLKFBIN 1	52	CLK 1
5	FAST 2	6	FAST 3	53	CLK 2
7	LOCKOUT 1	8	ROENX	54	
9	RWENX	10	CSU9X	55	
11	SEEP_SK	12	IO204CUS	56	
13	ASP_DT	14	ASP_DR	57	
15	RD 10	16	RD 11	58	
17	GND	18		59	GND
19	RD 9	20	RD 8	60	VCC_IO
21	RD 12	22	RD 13	61	
23	SEEP_DO	24	SEEP_CSX	62	
25	RD 14	26	RD 15	63	
27	RA 16	28	RA 15	64	
29	RRA 18	30	CSU10X	65	
31	RL 31	32	RL 1	66	
33	GND	34		67	GND
35	RA 9	36	RA 12	68	VCC_AUX
37	RA 11	38	RA 10	69	
39	RA 13	40	RA 8	70	
41	RA 17	42	RA 14	71	
43	ASP_INT	44	CS_ROMX	72	
45	ASP_RCLK	46	ASP_TCLK	73	
47	ASP_TFS	48	ASP_RFS	74	
49	GND	50		75	GND

APEX 20K Signal List

Signal	APEX Pin	Connector	Pin
ASP_DR	170	P4	14
		P5	15
ASP_DT	171	P4	13
		P5	13
ASP_INT	174	P4	43
		P5	3
ASP_RCLK	180	P4	45
		P5	7
ASP_RFS	173	P4	48
		P5	11
ASP_TCLK	172	P4	46
		P5	5
ASP_TFS	178	P4	47
		P5	9
A_OEX	4		
A_RCV	8		
A_SUSP	10	P2	45
A_VM	3	P2	47
A_VMO	2	P2	23
A_VP	9	P2	39
A_VPO	7	P2	43
CDAT	153	P2	14
		P8	9
CLK0	31	P2	53
CLK1	151	P4	52
CLK2	34	P2	52
CLK3	154	P4	53
CLKFBIN0	35	P2	4
CLKOUT0	23	P2	2
CLKOUT1	139	P4	2
CONFDONE	93	P8	3
CSU7X	80	P1	5
CSU8X	115	P3	14
CSU9X	223	P4	10
CSU10X	237	P4	30
CS_ROMX	239	P4	44
DCLK	152	P8	1

Signal	APEX Pin	Connector	Pin
DIG1	46	P1	47
DIG2	62	P1	42
DIG3	54	P1	37
DIG4	59	P1	31
FAST0	212	P2	6
FAST1	209	P2	5
FAST2	88	P4	5
FAST3	91	P4	6
IO124	124	P3	44
IO125	125	P3	39
IO126	126	P3	42
		P4	11
IO130	130	P3	46
IO131	131	P3	40
IO133	133	P3	41
IO134	134	P3	37
IO143DOE	143	P2	7
IO156DCL	156	P2	8
IO157CS	157	P2	12
IO160NCS	160	P2	11
IO161NRS	161	P2	10
IO164NWS	164	P2	9
IO166	66	P3	38
IO204CUS	204	P4	12
IO205RDY	205	P2	13
IO206IDO	206	P2	16
KEY_S1	61	P1	41
KEY_S2	50	P1	40
KEY_S3	63	P1	39
KEY_S4	57	P1	30
LA0	77	P1	6
LA1	75	P1	7
LA2	71	P1	8

APEX 20K Signal List

Signal	APEX Pin	Connector	Pin
LA3	69	P1	9
LA4	68	P1	15
LA5	70	P1	14
LA6	74	P1	13
LA7	76	P1	12
LA8	96	P3	6
LA9	99	P3	8
LA10	101	P3	10
LA11	103	P3	22
LA12	105	P3	23
LA13	109	P3	11
LA14	104	P3	12
LA15	102	P3	9
LA16	100	P3	7
LA17	119	P1	10
LA18	110	P3	13
LD0	111	P3	16
LD1	112	P3	15
LD1_GN	48	P1	45
LD1_RT	47	P1	46
LD2	113	P3	19
LD2_GN	53	P1	43
LD2_RT	49	P1	44
LD3	114	P3	20
LD3_GN	65	P1	35
LD3_RT	64	P1	38
LD4	121	P3	24
LD4_GN	58	P1	32
LD4_RT	55	P1	36
LD5	116	P3	21
LD6	117	P3	26
LD7	118	P3	36
LD8	82	P1	19
LD9	84	P1	16
LD10	85	P3	25
LD11	95	P3	30

Signal	APEX Pin	Connector	Pin
LD12	94	P3	32
LD13	123	P3	29
LD14	83	P1	20
LD15	81	P1	21
LOCKOUT0	40	P2	20
LOCKOUT1	138	P4	7
LOCKOUT2	20	P2	15
LOCKOUT3	135	P3	47
LOENX	79	P1	11
LWENX	98	P3	5
MSEL0	29		
MSEL1	30		
NCE	150		
NCEO	213		
NCONFIG	33	P8	5
NSTATUS	92	P8	7
NTRST	214		
RA0	192	P2	26
RA1	196	P2	27
RA2	201	P2	28
RA3	183	P2	25
RA4	215	P2	30
RA5	197	P2	41
RA6	225	P2	42
RA7	231	P2	44
RA8	224	P4	40
RA9	232	P4	35
RA10	202	P4	38
RA11	230	P4	37
RA12	234	P4	36
RA13	226	P4	39
RA14	233	P4	42
RA15	198	P4	28
RA16	203	P4	27
RA17	236	P4	41
RRA18	191	P4	29

APEX 20K Signal List

Signal	APEX Pin	Connector	Pin
RD0	182	P2	29
RD1	200	P2	32
RD2	195	P2	31
RD3	189	P2	36
RD4	185	P2	37
RD5	181	P2	38
RD6	169	P2	35
RD7	166	P2	40
RD8	221	P4	20
RD9	219	P4	19
RD10	216	P4	15
RD11	187	P4	16
RD12	207	P4	21
RD13	186	P4	22
RD14	217	P4	25
RD15	220	P4	26
RL1	238	P4	32
RL31	235	P4	31
ROENX	222	P4	8
RWENX	190	P4	9

Signal	APEX Pin	Connector	Pin
SEEP_CSX	184	P4	24
SEEP_DI	136	P3	48
SEEP_DO	163	P4	23
SEEP_SK	129	P3	45
		P4	11
SEG_A	13	P1	25
SEG_B	11	P1	27
SEG_C	18	P1	22
SEG_D	41	P1	24
SEG_DP	43	P1	28
SEG_E	44	P1	26
SEG_F	16	P1	23
SEG_G	17	P1	29
TCK	87	P1	54
		P6	1
		P7	1
TDI	149		
TDO	208	P7	9
TMS	86	P1	55
		P6	5
		P7	5