El Camino
Training - Engineering - Consultancy

AES/SPDIF Transmitter

AES/EBU Transmitter
VHDL Core

Version: 1.0

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Functional Description

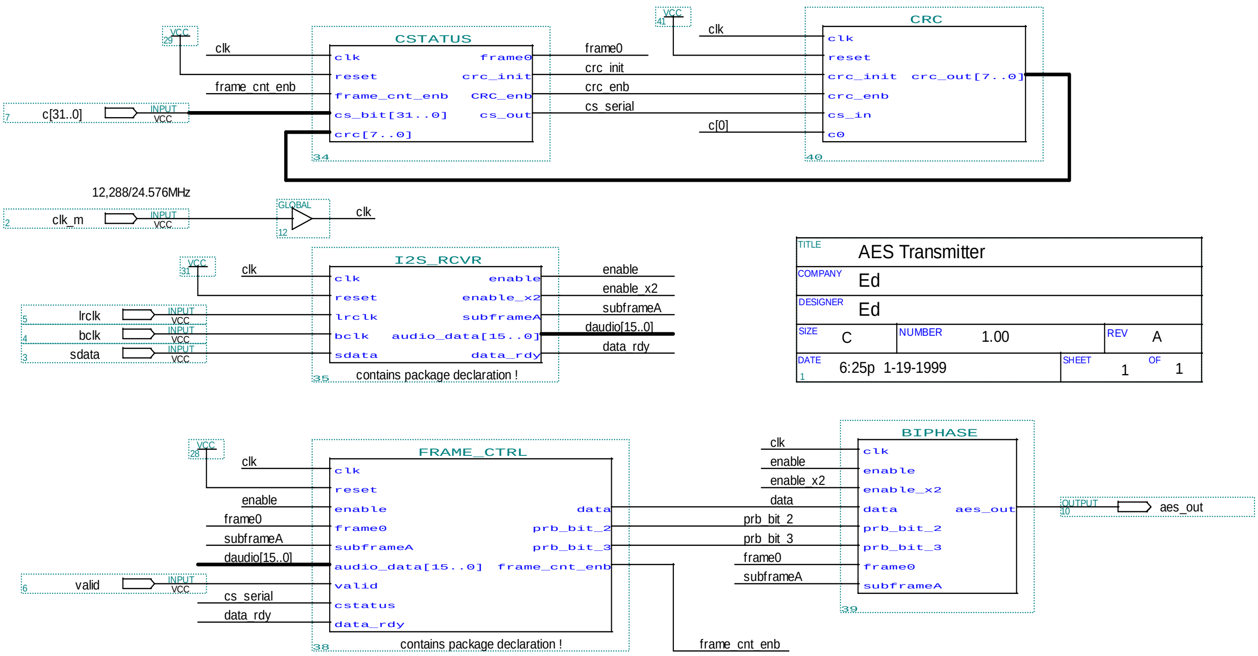
This core is a **synchronous** AES/EBU transmitter for digital audio. The features are similar to the CS8402A except that the design is fully synchronous. The serial output is coupled to the serial input whereas in the CS8204A it is not. See appendix A for details. The core supports channel status in a frame of 192 bits. Only the first 32 bits are implemented to keep the gate count low. CRC is automatically switched of if C0 is „zero“ for consumer mode. The CRC block can be left out completely as can be seen in the top level sheet of SPDIF.gdf below . Auxiliary and User data are also left out. Validity and Parity are active in all modes.

The design is **scalable**. It supports a master clock of 256 or 512 times f_sample. The word length can be anything from 16 to 24 bits. Sample rates can vary from 32kHz to 96kHz even with low speed grade FPGAs.

On of the most important differences regarding other cores or chips is the fact that there are **no state machines** that have to be reset. All the counters in the design are set or reset periodically by the I2S input. There are no „dead states“. This gives 100% stability and reliability to the core. Even asynchronously switching the master clock from 11.2986MHz to 12.288MHz f.e. can not „hang up“ the design.
The cell count is around 190 LCELLs in an EPF10K10 design including CRC and 32 fully programmable channel status bits. SPDIF is around 150. Tying some of the status bits to zero or one saves even more LCELLs.
The DIGILAB 10K10 or other DIGILAB boards can be used for evaluation and prototyping.

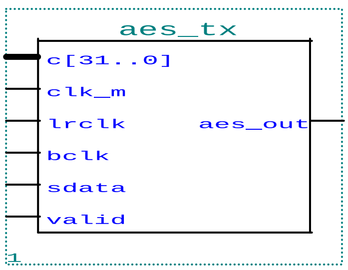
The top level is named **“AES_TX.VHD”** and is shown here as Altera “GDF” sheet for reference. The source code is fully commented in English. There’s a VHDL package included **“AES_TX_PGK.VHD”** that can be modified to change the word length and clock rate will be provided. This package is not encrypted. **It is necessary to select this package as a project and do a “Save & Check” before the “AES_TX” function can be compiled.**

Top Level Sheet – AES.GDF



I/O Ports

- CLK_M is the master clock of 256 or 512 times f_sample.
- C[31..0] are the channel status bits from 0 to 31.
- LRCLK is the word sync of the I2S input.
- BCLK is the bit clock of the I2S input.
- SDATA is the serial data input of the I2S input.
- VALID is the input that controls the validity bit in every sub frame.
- AES_OUT is the bi-phase output that feeds the high current driver for the SPDIF or AES compatible output.



Timing

The input timing of the I2S receiver is slightly different then the CS8402A in the sense that it is synchronous regarding to the master clock. BCLK is not anymore a real clock that runs to the clock node of internal flip flops. It is instead implemented as a qualifier. The rising edge i.e. the first time BCLK is sampled high by the master CLK_M after being low for at least one clock cycle is also the moment when SDATA and LRCLK are sampled. This approached was considered the most straight forward to implement and describe. Timing can be changed easily by adding one flip flop before BCLK or SDATA and LRCLK.

All inputs and outputs are direct inputs or outputs of D-type flip flops. This simplifies timing issues between the AES core and other parts of the ASIC or PLD.

APENDIX A

Synchronous versus Asynchronous

If you look at the data sheet of the CS8204A you will find a block drawing of the internal structure in figure B1, Appendix B. It shows two shift registers and an intermediate parallel audio buffer. The reason for the presence of the intermediate register is the following: The serial audio input can contain jitter depending which source it comes from. A typical case is when a AES transmitter follows an AES receiver in a circuit that runs on the clock provided by the receiver. If the master clock (MCK) supplied to the transmitter is restored by a VCXO based PLL for example there will be jitter between the bit clk (SCK) and MCK.
To avoid synchronization problems SCK is not sampled by MCK. In fact SCK drives the shift in register and the audio buffer and MCK drives the shift out register and the rest of the AES framing state machine. Crystal is aware of the problem that arises when the transfer into and out of the audio buffer overlap and provides a reset circuit to change the phase of the subframe counters if this overlap occurs.
The absolute phase between the I2 frames and the AES subframes depends on the situation after reset and is therefore random. The user has no way to know how close to an overlap reset his circuit is at any moment. A spike in the phase noise can cause a reset any time.
Obviously it is still mandatory that SCK and MCK are locked over time otherwise periodical resets would cause drop outs in the AES signal. Besides that a full blown sample rate conversion would be needed.

In an circuit where BCLK, SDATA and LRCLK are generated synchronous to the master clock all this can be left out. The supplied core does not contain the audio buffer between the shift registers. The shift out register is loaded and the respective counters are reset when the last bit (LSB) of the I2S stream has arrived in the shift in register. The delay between the I2 frames and the AES subframes is constant and depends only on the word length that was chosen in the constant declarations of the VHDL source code.
But the biggest advantage of a synchronous design is the possibility to control the whole „machine" by the edge of LRCLK. No reset is needed and no hang ups can happen.

Deliverables

- Encrypted gate level netlist optimised for Altera's FLEX®/APEX™ architectures

alternative

- VHDL source code