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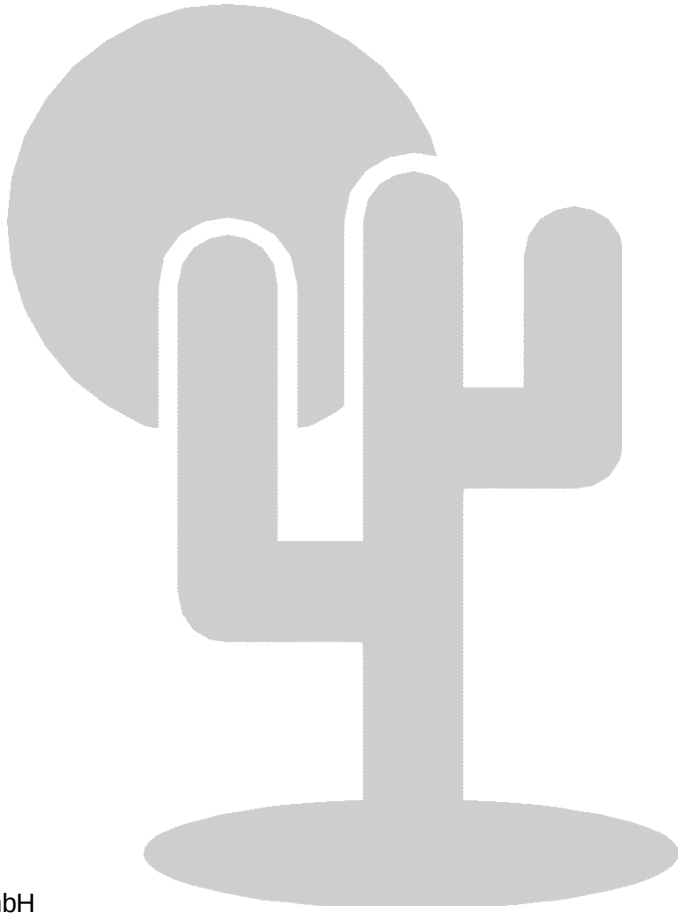
DIGILAB 10Kx240 MANUAL

FLEX® 10K Prototyping System



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Chapter

1

Digilab 10Kx240 – Preface

General Description

The DIGILAB 10Kx240 is intended for prototyping based on Altera's FLEX 10K devices. It supports all FLEX 10K devices in the QFP240 package (including A-,V-,S- and E-families).

DIGILAB 10Kx240 Features:

- Comes with your choice of FLEX 10K device in (R)QFP 240 package (FLEX 10K, FLEX 10KA, FLEX 10KV, FLEX 10KE or FLEX 10KS)
- 58-178 User I/Os (depends on which on-board functions are used)
- 4-Layer PCB in Europe-Standard format
- 1-2 Configuration Flash EPROMs EPC2 on board
- Bi-colour status LED for STATUS, CONFDONE
- Debounced reboot/reset push buttons
- JTAG-Input/-Output for Cascading multiple Modules
- Insertion Slots for either one sub-module in Europe-Standard format or two individual sub-modules in half the size
- Three individual operating voltages (VCC-IO, VCC-INT, VCC-AUX) @ 5V, 3.3V and 2.5V
- Two individual independent SRAM Banks with 512kx16 each fast SRAM
- Optional socket for 28DIL or 32DIL (EE/E)PROM
- Driver and connector for serial interface
- Optional quarz oscillator, rectangular or squared outline
- PLL support
- 4-digit, multiplexed 7- segment display
- Four bicolor LEDs
- Four pushbuttons
- Connector for interfacing with DSP (e.g. SHARC-DSP-Eazy-Kit) SPORT- or LINK-Interface as an option

Warning:
This is a class A device. This device may cause radio interference in the living area.
The user may be required to carry out and be responsible for appropriate measures.

Chapter
2

Board Description

Disable Functions and Reserve Inputs

In order to avoid contention on the board make sure you follow the following guidelines. Disabling on-board functions also allows the use of associated signals for your own, custom applications.

1. Disable all functions that are not required

Function	To Disable	Signal Name	FLEX 10K Pin
Memory Bank 0 (left), LSB	drive high	CSU8X	55
Memory Bank 0 (left), MSB	drive high	CSU7X	19
Memory Bank 1 (right), LSB	drive high	CSU10X	128
Memory Bank 2 (right), MSB	drive high	CSU9X	129
(EE)PROM (optional)	drive high	CS_ROMX	131
Serial EEPROM, U5	drive high	SEEP_CSX	127
Serial Interface, U11	drive high	SER_EN	191

2. Implement Inputs in your design for those functions that can't be disabled

Function	To Disable	Signal Name	FLEX 10K Pin
Push Button S1	reserve input	KEY_S1	215
Push Button S2	reserve input	KEY_S2	229
Push Button S3	reserve input	KEY_S3	230
Push Button S4	reserve input	KEY_S4	234

3. Some pins that are VCC or GND pins in larger FLEX 10K devices are general purpose user I/Os in smaller devices. These pins are connected to VCC or GND on the DIGILAB 10Kx240 in order to support the largest device in QFP 240. Such pins are listed in the table on the next page and need to be reserved as unused inputs in your design.

Always Reserve these Pins as Unused Inputs

Function in larger devices	FLEX 10K Pin	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70		EPF10K30A	EPF10K50V	EPF10K100A		EPF10K50S	EPF10K100E	EPF10K130E	EPF10K200S
VCC_INT	20	X	X	X	X	X		X	X	X		X	X		
	40	X	X	X	X	X		X	X	X		X	X	X	
	76	X	X	X	X	X		X	X	X		X	X		
	139	X	X	X	X	X		X	X	X		X	X	X	
	159	X	X	X	X	X		X	X	X		X	X		
	187	X	X	X	X	X		X	X	X		X	X	X	
	225	X	X	X	X	X		X	X	X		X	X	X	

X pin is driven on the board, reserve as unused input in your design!

MultiVolt Support

Only some FLEX 10K devices in (R)QFP 240 pin packages support MultiVolt. You must not implement different VCC_INT and VCC_IO voltages for those devices that don't support MultiVolt!

FLEX 10K Device	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70		EPF10K30A	EPF10K50V	EPF10K100A		EPF10K50S	EPF10K100E	EPF10K130E	EPF10K200S
MultiVolt Support											X	X	X	X

NEVER USE DIFFERENT VCC_INT AND VCC_IO FOR THOSE DEVICES THAT DON'T SUPPORT MULTIVOLT! DOING SO WILL DAMAGE THE DEVICE!

Voltage Regulators and Power Supply

There are three voltage regulators on the board (VCC_INT, VCC_IO, VCC_AUX). Depending on the device they may be set to different voltages.

VCC_INT is the internal voltage of the FLEX device. This voltage is fixed and not user-selectable. VCC_INT is generated by the regulator U5.

	FLEX 10K	FLEX 10KA/V	FLEX 10KB/E/S
VCC_INT (fixed)	5 V	3.3 V	2.5 V

VCC_IO is the supply-voltage for the FLEX-IOs and can also be used to supply some on board devices such as the Memory, serial interface etc. VCC_IO is generated by U6. You can select between two different fixed values just by connecting or disconnecting JP5.
NEVER USE A VCC_IO THAT DIFFERS FROM VCC_INT FOR THOSE DEVICES THAT DON'T SUPPORT MULTIVOLT (SEE TABLE ON PREVIOUS PAGE). DOING SO WILL DAMAGE THE DEVICE!

	JP5					
	FLEX 10K		FLEX 10KA/V		FLEX 10KB/E/S	
	open	closed	**open**	closed	**open**	closed
VCC_IO	**5.0 V**	3.3V	**3.3 V**	2.5 V	**3.3 V**	2.5 V

default values in bold

VCC_AUX is an additional supply voltage that you may use in your application. It is generated by U14. You can select between two different fixed values by connecting JP2. As a default setting none of the on-board devices use VCC_AUX.

	JP2	
	open	**closed**
VCC_AUX	5.0 V	**3.3 V**

default values in bold

The following table shows the limits (minimum and maximum) for the input voltage of the board. Please consider that an input voltage much above the maximum value will cause excessive heat on the board.

	V_{IN} MIN	V_{IN} MAX
any V_{CC} = 5 V	7.5 V	12.0 V
all $V_{CC} \leq$ 3.3 V	5.8 V	12.0 V

Maximum/Minimum Input Voltage

The required current will depend largely on your design and the clock frequency.

Configuration

There are four different ways to configure the FLEX device:

1. Configuration via JTAG-Interface
2. From the EPC2
3. Parallel mode
4. Serial mode from an external processor

Description of the JTAG-Chain:
To setup the JTAG-Chain properly you need to consider the following details. The JTAG-chain starts at P1. Normally, a Byte-Blaster, Master-Blaster or the output of another board is connected to this plug.

You have the possibility to feed the JTAG chain to your own devices on the daughter board 1. Therefore the JTAG-signals feeds to P5B where you can insert your own JTAG-capable devices in the chain.
If you don't use this feature or no daughter board is used at all you need to connect the signal TDI with TDI_EPC. Setting the jumper JP5 will do this for you (default setting).

The JTAG-chain is then connected to the first (U2) and second (U3) EPC2 device. Depending on the type of APEX-device there are one or two EPC2 on your board. If only one device is required it must be installed on U2 and the jumper JP6 must be installed.

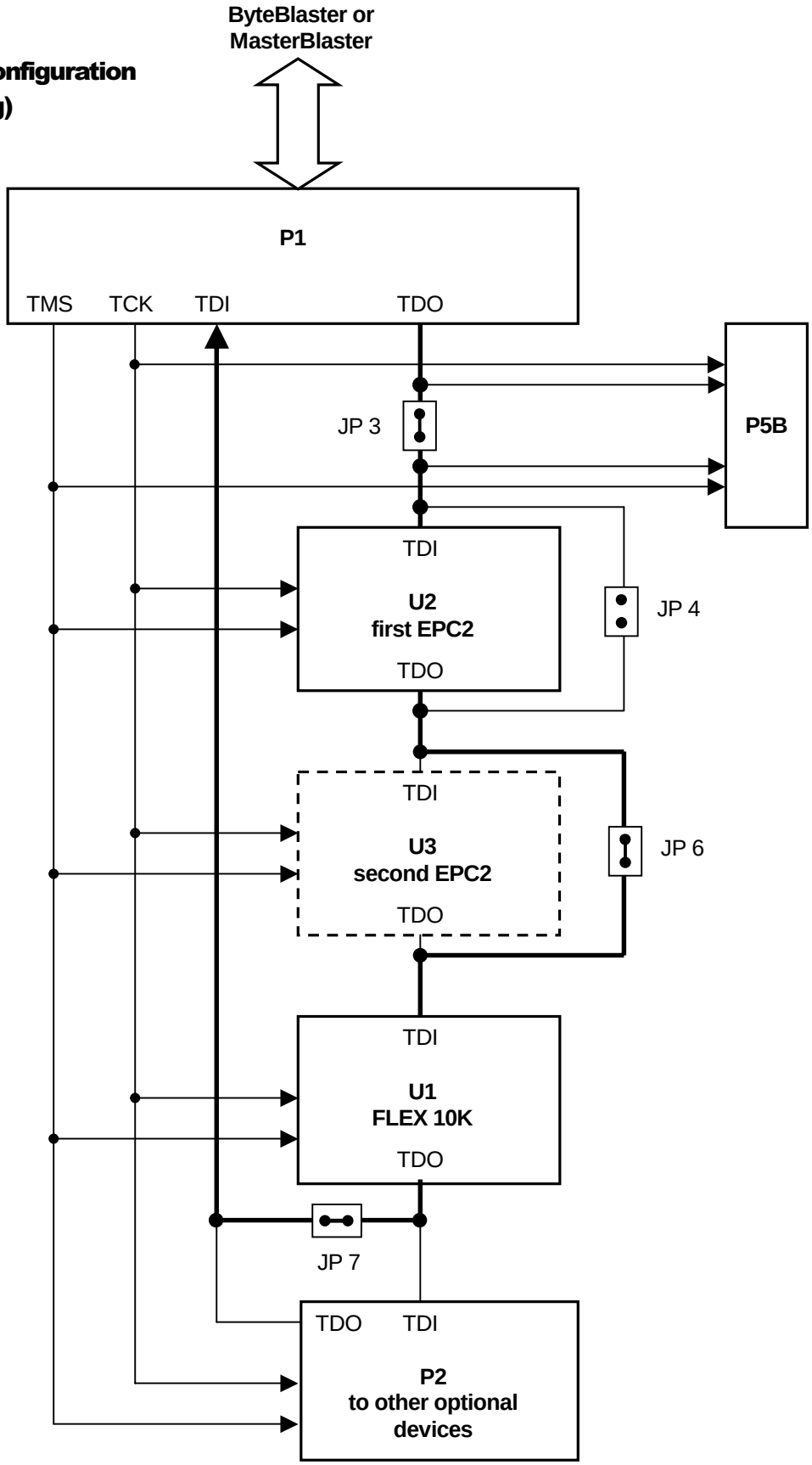
Next, the JTAG chain feeds the FLEX-device and goes on to P2. It allows to connect additional boards to your JTAG chain. If you don't need this feature, JP7 must be installed (default).

The JTAG-chain in the programmer window needs to be setup in the same order as it is physically implemented on the board:

(Devices on daughter board, optional) => first EPC2 (U2) => second EPC2 (U3, if required) => FLEX device => (additional devices on another board connected to P2, optional).

The picture on the next page shows a block diagram of the JTAG chain

JTAG Chain Configuration
(default setting)



When you have finished the setup you should check the chain with your configuration software MAX+plus II. Now you are ready to either configure the FLEX and/or program the EPC2(s) via the JTAG-Interface.

Once you have programmed the EPC2s the FLEX-device configures itself every time the board is powered up. You can force a reconfiguration either with a JTAG-command which is executed by U2 or U3, via S6 (reconfigure button), by downloading a new configuration or re-programming the EPC2s (U2, U3).

LED5 is connected to the CONF_DONE and NSTATUS outputs of the FLEX 10K device and gives you the status of the configuration.

		LED 5
Configuration Error	NSTATUS = low	red
Configuration Successful	CONF_DONE = high	green

If you want to use the parallel-mode configuration you can easily access all necessary signals via connector P6A. For parallel configuration, BR1 and BR2 (MSEL0 and MSEL1 inputs) must be changed properly. Per default they are set to serial configuration.

To implement a serial configuration performed form an alternative device (e.g. a microprocessor) instead of the EPC2s, both EPC2s (U2, U3) need to be removed. You can then use P8 to connect your own signals (DCLK, DATA0, CONF_DONE, NSTATUS, NCONFIG).

Global Reset

There is a global reset switch (S5) which feeds the global reset input (DEV_CLRn) of the FLEX device. This switch is already debounced to avoid problems. If you want to use the global reset feature it must be enabled in the Device Settings in the Compiler.

Memory

There are two independent banks of memory (memory bank0/left, memory bank1/right), each up to 512K by 16. Independent means that there are separate address-, data- and control-lines for each of the banks. It enables the FLEX device to access both memories in one clock-cycle with independent addresses and data. This is useful for e.g. FFT-applications. Nevertheless, connecting the addresses internally enables also building a single wide (32 Bit) memory for other applications.

If specific applications require only one memory bank or no external memory at all, the according CSx-lines should be pulled to a logic high level. The memory is then inactive and you can use the IO-ports of the FLEX device for other purposes

The supply-voltage of both memories can be chosen independently via BR8 (bank0/left) and BR5 (bank1/right). Normally they should be connected to VCC_IO (default setting).

The right memory bank shares it's data lines with the data lines required for configuration in parallel mode (except D0). This is useful because the lower data lines of the microprocessor have to be connected to this IOs when you use this configuration mode.

In addition, the right memory bank has a socket for a standard ROM, PROM, (E)EPROM or FLASH device in a 28/32 pin DIL standard JEDEC package. Some pins (RL1, RL31) which have different function depending on the type of device being used, are fed to the FLEX separately. The remaining addresses and data lines are shared with the right RAM bank.

The supply voltage can be selected separately via BR14 for this device. BR15 selects between 28 or 32 pin device. You need to take care about the voltage compatibility between the device and the according FLEX IO-pins.

		Chip Select	drive to	FLEX 10K Pin
Memory Bank 0 (left)	LSB	CSU8X	high	55
	MSB	CSU7X	high	19
Memory Bank 1 (right)	LSB	CSU10X	high	128
	MSB	CSU9X	high	129
(EE)PROM (optional)	LSB	CS_ROMX	high	131

Disable Memory

Serial EEPROM

There is serial EEPROM (93C46A) on the board. This device can be used to store some user defined, nonvolatile data. For a description and the protocol (serial read and write) please refer to the 93C46A datasheet e.g. from Atmel.

If you don't use this device just make sure to pull the signal SEEP_CSx to a logic high level. The other signals connected to the device can then be used as FLEX 10K user-IOs.

		Chip Select	drive to	FLEX 10K Pin
Serial EEPROM	U13	SEEP_CSX	high	127

Disable Serial EEPROM

Serial Interface

The DIGILAB 10Kx240 has a RS232 driver (ADM3222, U11) and according 9-pin connector on board.

If you don't need the serial interface functionality you may drive SER_EN to a logic high level. By doing so, you can use all other FLEX 10K IO-pins associated with the serial interface as regular user-IOs.

ADSP-SPORT Interface

P9 can be used as high speed interface for connecting different other devices. Originally, it was designed to connect to the SPORT of an ADSP-SHARC Board. Nevertheless, it can also be used in other similar applications where a flat cable must be used because of it's defined impedance. On this connector a signal line is always surrounded by GND-lines.

An optional termination network (RN07) can be added.

Display and Switches

There is a 4-digit 7-segment multiplexed display on the board. A display driver macrofunction can be found on the web (http://www.elca.de).

Furthermore, there are 4 LEDs each capable of displaying two independent colors (red/green) and 4 push buttons. Please keep in mind that these buttons are not de-bounced. An example of a de-bouncing circuitry can also be found on the web-site.

If you don't need this functionality you can just disconnect the supply for these devices (BR13 for the Display, BR12 for the LEDs).

Module Connectors and Daughter Boards

All relevant signals of the FLEX device are accessible via 4 connectors, two on each side of the board (P3, P4, P5, P6).

Each connector itself consists of two parts. One is a 2 by 25 connector with a shell. This part allows to plug in a flat-wire connector or daughter board. In addition, there is another 25 pin connector (single line) which contains some auxiliary signals. Many pins of this connector are not populated which allows you to route your own signals to these pins.

You can plug in daughter boards with your specific circuitry. One of these daughter boards (with prototyping area) can be purchased from El Camino.

Two small or one large board can be connected.

P6 contains all signals that are needed for parallel configuration and the lower 8 address- and 8 data lines for the right memory block,

P4 contains the rest of the address- and data-lines of the right memory bank.

P5 contains parts of the left memory bank signals and the display/button control signals, P3 the rest of the left memory-bank signals.

96-Pin-Edge Connector (Optional)

There is additional board space for an optional 96/64-pin connector. By default no signals of the board are routed to this connector. It may be useful if you need to place the board into a 19" rack with a back plane connector.

It's only possible to use this connector while no serial interface and no ADSP-SPORT interface connectors are present.

Clock Generation and PLL Support

There is a quartz-oscillator on board (default 48MHz) which can drive CLK1. Instead of the quartz-oscillator the master clock can be fed via J6 (optional). In case of using J6 the oscillator must be removed. All clock-signals on the board have a defined impedance of 50 ohm (stripeline). Optionally, the clocks can be terminated close to the clock pin of the FLEX device (R19/C63 for CLK1, R20/C62 for CLK2).

	Resistor	Capacitor
CLK 0	R 19	C 63
CLK 1	R 20	C 62

Optional Clock Termination

CLK0 and CLK1 can be fed either by …….. or by JP1, JP8. Unused clock pins must be tied to a fixed level (GND or VCCIO). This can be done by setting the jumpers JP1 and/or JP8.

Depending on the device installed there is a PLL available

The power supply for the PLLs is critical (affects jitter), therefore the PLL supply is decoupled via a L/C combination.

There is also one special indicating the lock-state of the according PLL (IO73/LOCK, Pin 73 of the FLEX 10K device).

Jumpers

Jumper	Description	open	closed
JP 1	Clock 0 Select	■ Clock from Connector	Clock from Oscillator
JP 2	VCC-AUX voltage	VCC-AUX = high voltage	■ VCC-AUX = low voltage
JP 3	JTAG-Chain to daughter board 1	Daughter board present	■ Daughter board not present
JP 4	JTAG-Chain, no U2 (EPC2)	■ First EPC2 present	First EPC2 not present
JP 5	VCC-IO voltage	■ VCC-IO = high voltage	VCC-IO = low voltage
JP 6	JTAG-Chain, no U3 (second EPC2)	Second EPC2 present	■ Second EPC2 not present
JP 7	JTAG-Chain, connect to next board	JTAG chain continues on next board	■ JTAG chain doesn't continue on next board
JP 8	Clock 1 Select	Clock input driven	■ Clock input connected to GND

■ default setting

Bridges

Bridge	Description	A-X or closed	B-X
BR 1	U1, MSEL 0	GND	VCC_IO
BR 2	U1, MSEL 1	GND	VCC_IO
BR 3	EPC2, VPP select	GND	VCC_EPC (see BR 7)
BR 4	EPC2, VCC select	GND	VCC_EPC (see BR 7)
BR 5	Memory Bank 1, right, VCC select	VCC_IO	VCC_AUX
BR 6	Clock 0 to connectors	connected	
BR 7	VCC_EPC select	VCC_IO	VCC_AUX
BR 8	Memory Bank 0, left, VCC select	VCC_IO	VCC_AUX
BR 9	VCC_OSC select	VCC_IO	VCC_AUX
BR 10	VCC_SER select	VCC_IO	VCC_AUX
BR 11	VCC_BY select	VCC_IO	VCC_AUX
BR 12	VCC_LED select	VCC_IO	VCC_AUX
BR 13	VCC_SEG select	VCC_IO	VCC_AUX
BR 14	VCC_ROM select	VCC_IO	VCC_AUX
BR 15	ROM (U6), address A17	RA17 (FLEX I/O)	VCC_ROM
BR 16	JTAG out (P2), VCC	VCC_BY	
BR 17	Serial Configuration (P8), VCC	VCC_BY	
BR 18	VCC_INT – VCC_IO connect	VCC_INT - VCC_IO connected	

■ default setting

User Connector Counting

P5A P6A

2	4	6	8	10	12				46	48	50
□1	3	5	7	9	11				45	47	49

P5B P6B

51	52	53	54	55	56				73	74	75

□ Square pad on bottom side marks pin 1

P3B P4B

51	52	53	54	55	56				73	74	75

P3A P4A

2	4	6	8	10	12				46	48	50
□1	3	5	7	9	11				45	47	49

□ Square pad on bottom side marks pin 1

User Connector Pinout P3

P3A				P3B	
1	GND	2		51	GND
3		4		52	
5	LWENX	6	LA8	53	
7	LA16	8	LA9	54	
9	LA15	10	LA10	55	
11	LA13	12	LA14	56	
13	LA18	14	CSU8X	57	
15	LD1	16	LD0	58	
17	GND	18		59	GND
19	LD2	20	LD3	60	VCC_IO
21	LD5	22	LA11	61	
23	LA12	24	LD7	62	RECONFSW
25	LD10	26	LD6	63	
27	IO88	28	LD4	64	IO83
29	LD13	30	LD11	65	GCLRSW
31	IO63	32	LD12	66	IO87
33	GND	34		67	GND
35	IO66	36	IO64	68	VCC_AUX
37	IO75	38	IO74	69	IO70
39	IO80	40	IO79	70	IO78
41	IO82	42	IO81	71	IO86
43	IO68	44	IO67	72	IO65
45	IO73	46	IO72	73	IO71
47	IO84	48	C91_CONN	74	C91_CONN
49	GND	50		75	GND

User Connector Pinout P4

P4A				P4B	
1	GND	2		51	GND
3		4	C91_CONN	52	C91_CONN
5	I90	6	I92	53	
7	IO110	8	IO111	54	IO101
9	IO100	10	IO99	55	IO102
11	IO98	12	IO97	56	IO103
13	IO95	14	IO94	57	IO105
15	RD10	16	RD11	58	IO106
17	GND	18		59	GND
19	RD9	20	RD8	60	VCC_IO
21	RD12	22	RD13	61	IO107
23	SEEP_DO	24	SEEP_DI	62	IO113
25	RD14	26	RD15	63	IO149
27	RA16	28	RA15	64	
29	RRA18	30		65	
31	RL31	32	RL1	66	
33	GND	34		67	GND
35	RA9	36	RA12	68	VCC_AUX
37	RA11	38	RA10	69	
39	RA13	40	RA8	70	
41	RA17	42	RA14	71	
43	ASP_DR	44	ASP_DT	72	
45	ASP_RCLK	46	ASP_TFS	73	
47	ASP_INT	48	ASP_TCLK	74	
49	GND	50		75	GND

User Connector Pinout P5

P5A				P5B	
1	GND	2		51	GND
3		4		52	
5	CSU7X	6	LA0	53	
7	LA1	8	LA2	54	TCK
9	LA3	10	LA17	55	TMS
11	LOENX	12	LA7	56	TDI
13	LA6	14	LA5	57	TDI_EPC
15	LA4	16	LD9	58	
17	GND	18		59	GND
19	LD8	20	LD14	60	VCC_IO
21	LD15	22	SEG_C	61	
23	SEG_G	24	SEG_D	62	
25	SEG_A	26	SEG_E	63	
27	SEB_B	28	SEG_DP	64	
29	SEG_F	30	LD4_RT	65	
31	DIG4	32	KEY_S4	66	
33	GND	34		67	GND
35	LD3_RT	36	LD4_GN	68	VCC_AUX
37	DIG3	38	IO11/CUS	69	
39	LD2_RT	40	LD3_GN	70	
41	KEY_S3	42	DIG2	71	
43	KEY_S2	44	LD1_RT	72	
45	LD2_GN	46	DIG1	73	
47	KEY_S1	48	LD1_GN	74	
49	GND	50		75	GND

User Connector Pinout P6

P6A				P6B	
1	GND	2		51	GND
3		4		52	
5	I210	6	I212	53	
7	IO213DOE	8	IO209DCL	54	
9	IO238NWS	10	IO236NRS	55	
11	IO240NCS	12	IO239CS	56	
13	IO23/RDY	14	CDAT	57	
15	IO157	16	IO26-IDO	58	
17	GND	18		59	GND
19	IO202	20	IO151	60	VCC_IO
21	IO200	22	IO201	61	
23	IO198	24	IO199	62	
25	RA3	26	RA0	63	
27	RA1	28	RA2	64	
29	RD0	30	RA4	65	
31	RD2	32	RD1	66	
33	GND	34		67	GND
35	RD6	36	RD3	68	VCC_AUX
37	RD4	38	RD5	69	
39	SER_SD	40	RD7	70	
41	RA5	42	RA6	71	
43	SER_RXD	44	RA7	72	
45	SER_RTS	46	SER_TXD	73	
47	SER_EN	48	SER_CTS	74	
49	GND	50		75	GND

FLEX 10K Signal List

Signal	FLEX Pin	Connector	Pin
ALP_DR	114	P4	43
		P9	15
ASP_DT	115	P4	44
		P9	13
ASP_INT	120	P4	47
		P9	3
ASP_RCLK	118	P4	45
		P9	7
ASP_RFS	116		
		P9	11
ASP_TCLK	119	P4	48
		P9	5
ASP_TFS	117	P4	46
		P9	9
C91	91		
C91_CONN	211		
		P3	48
		P3	74
		P4	4
		P4	52
C211	211		
CDAT	180	P6	14
		P8	9
CONFDONE	2	P8	3
CSU7X	19	P5	5
CSU8X	55	P3	14
CSU9X	129		
CSU10X	128		
CS_ROMX	131		
DCLK	179	P8	1
DIG1	220	P5	46
DIG2	221	P5	42
DIG3	228	P5	37
DIG4	235	P5	31
I90	90	P4	5
I92	92	P4	6
I210	210	P6	5

Signal	FLEX Pin	Connector	Pin
I212	212	P6	6
IO11/CUS	11	P5	38
IO23/RDY	23	P6	13
IO26/IDO	26	P6	16
IO63	63	P3	31
IO64	64	P3	36
IO65	65	P3	72
IO66	66	P3	35
IO67	67	P3	44
IO68	68	P3	43
IO70	70	P3	69
IO71	71	P3	73
IO72	72	P3	46
IO73	73	P3	45
IO74	74	P3	38
IO75	75	P3	37
IO78	78	P3	70
IO79	79	P3	40
IO80	80	P3	39
IO81	81	P3	42
IO82	82	P3	41
IO83	83	P3	64
IO84	84	P3	47
IO86	86	P3	71
IO87	87	P3	66
IO88	88	P3	27
IO94	94	P4	14
IO95	95	P4	13
IO97	97	P4	12
IO98	98	P4	11
IO99	99	P4	10
IO100	100	P4	9
IO101	101	P4	54
IO102	102	P4	55
IO103	103	P4	56
IO105	105	P4	57
IO106	106	P4	58

FLEX 10K Signal List

Signal	FLEX Pin	Connector	Pin
IO107	107	P4	61
IO110	110	P4	7
IO111	111	P4	8
IO113	113	P4	62
IO149	149	P4	63
IO151	151	P6	20
IO157	157	P6	15
IO198	198	P6	23
IO199	199	P6	24
IO200	200	P6	21
IO201	201	P6	22
IO202	202	P6	19
IO209DCL	209	P6	8
IO213DOE	213	P6	7
IO236NRS	236	P6	10
IO238NWS	238	P6	9
IO239CS	239	P6	12
IO240NCS	240	P6	11
KEY_S1	215	P5	47
KEY_S2	229	P5	43
KEY_S3	230	P5	41
KEY_S4	234	P5	32
LA0	17	P5	6
LA1	14	P5	7
LA2	12	P5	8
LA3	8	P5	9
LA4	7	P5	15
LA5	9	P5	14
LA6	13	P5	13
LA7	15	P5	12
LA8	35	P3	6
LA9	38	P3	8
LA10	41	P3	10
LA11	44	P3	22
LA12	46	P3	23
LA13	48	P3	11
LA14	45	P3	12

Signal	FLEX Pin	Connector	Pin
LA15	43	P3	9
LA16	39	P3	7
LA17	6	P5	10
LA18	49	P3	13
LD0	50	P3	16
LD1	51	P3	15
LD1_GN	203	P5	48
LD1_RT	223	P5	44
LD2	53	P3	19
LD2_GN	222	P5	45
LD2_RT	227	P5	39
LD3	54	P3	20
LD3_GN	226	P5	40
LD3_RT	233	P5	35
LD4	62	P3	28
LD4_GN	231	P5	36
LD4_RT	237	P5	30
LD5	31	P3	21
LD6	61	P3	26
LD7	56	P3	24
LD8	28	P5	19
LD9	25	P5	16
LD10	29	P3	25
LD11	34	P3	30
LD12	33	P3	32
LD13	30	P3	29
LD14	24	P5	20
LD15	21	P5	21
LOENX	18	P5	11
LWENX	36	P3	5
MSEL0	124		
MSEL1	123		
NCE	178		
NCEO	3		
NCONFIG	121	P8	5
NSTATUS	60	P8	7
NTRST	59		

FLEX 10K Signal List

Signal	FLEX Pin	Connector	Pin
RA0	134	P6	26
RA1	138	P6	27
RA2	143	P6	28
RA3	136	P6	25
RA4	137	P6	30
RA5	141	P6	41
RA6	164	P6	42
RA7	168	P6	44
RA8	163	P4	40
RA9	172	P4	35
RA10	144	P4	38
RA11	167	P4	37
RA12	174	P4	36
RA13	166	P4	39
RA14	173	P4	42
RA15	142	P4	28
RA16	146	P4	27
RA17	175	P4	41
RRA18	133	P4	29
RD0	184	P6	29
RD1	181	P6	32
RD2	182	P6	31
RD3	183	P6	36
RD4	185	P6	37
RD5	186	P6	38
RD6	188	P6	35
RD7	190	P6	40
RD8	161	P4	20
RD9	156	P4	19
RD10	152	P4	15
RD11	147	P4	16
RD12	148	P4	21
RD13	153	P4	22
RD14	154	P4	25
RD15	158	P4	26

Signal	FLEX Pin	Connector	Pin
RL1	171	P4	32
RL31	169	P4	31
ROENX	162		
RWENX	132		
SEEP_CSX	127		
SEEP_DI	109	P4	24
SEEP_DO	108	P4	23
SEEP_SK	126		
SEG_A	217	P5	25
SEG_B	219	P5	27
SEG_C	208	P5	22
SEG_D	207	P5	24
SEG_DP	206	P5	28
SEG_E	204	P5	26
SEG_F	214	P5	29
SEG_G	218	P5	23
SER_CTS	193	P6	48
SER_EN	191	P6	47
SER_RTS	194	P6	45
SER_RXD	196	P6	43
SER_SD	192	P6	39
SER_TXD	195	P6	46
TCK	1	P1	1
		P2	1
		P5	54
TDO_EPCB	177		
TDO_FL	4	P2	9
TMS	58	P1	5
		P2	5
		P5	55
TDI_EPC		P5	57