El Camino
Training - Engineering - Consultancy

DIGILAB SX III

Stratix III Prototyping Board

General Description

The DIGILAB SX III is a universal FPGA prototyping platform based on Altera's Stratix III device family. It can be used for ASIC prototyping, hardware evaluation or as a verification accelleration vehicle

Features

- Available with any Altera Stratix III device in 1517 Pin FineLine BGA Package and at least 960 IOs
  - EP3SE260
  - EP3SL340
- 353 user I/Os through
  - Three 120 pin Samtec connectors
  - One 60 pin Samtec connector
  - Two 38 pin Mictor connectors
  - Four 16 pin DIL headers
- 2 MByte (512k x 32-bit) FLASH memory
- 2 MByte (512k x 32-bit) SRAM
- Configuration
  - EPCS128 non-volatile configuration memory
  - Push-buttons for reset and configuration
  - Various LEDs for configuration status
- User Interface
  - 32 three-state DIP switches with programmable pull-up/pull-down and 32 user LEDs
  - 16 two-state DIP switches
  - 8 push buttons, selectable low- or high active with programmable pull-up/pull-dow
- Connector for SD/MMC cards
- JTAG connector for Altera download cable
- JTAG Multi-ICE connector
- Interfaces with monitoring LEDs
  - Two RS232 transceivers with 3-driver/3-receiver each
  - SPI interface connector
  - USB 1.1 transceiver (USB 2.0 support on request)
- Clocking
  - 80 MHz Crystal oscillator
  - 20 MHz Temperature compensated crystal oscillator (optional)
  - 3 SMA clock inputs
- Power supply circuitry
- FPGA controlled active heat sink and temperature sensor

Preface

Environmental Requirements

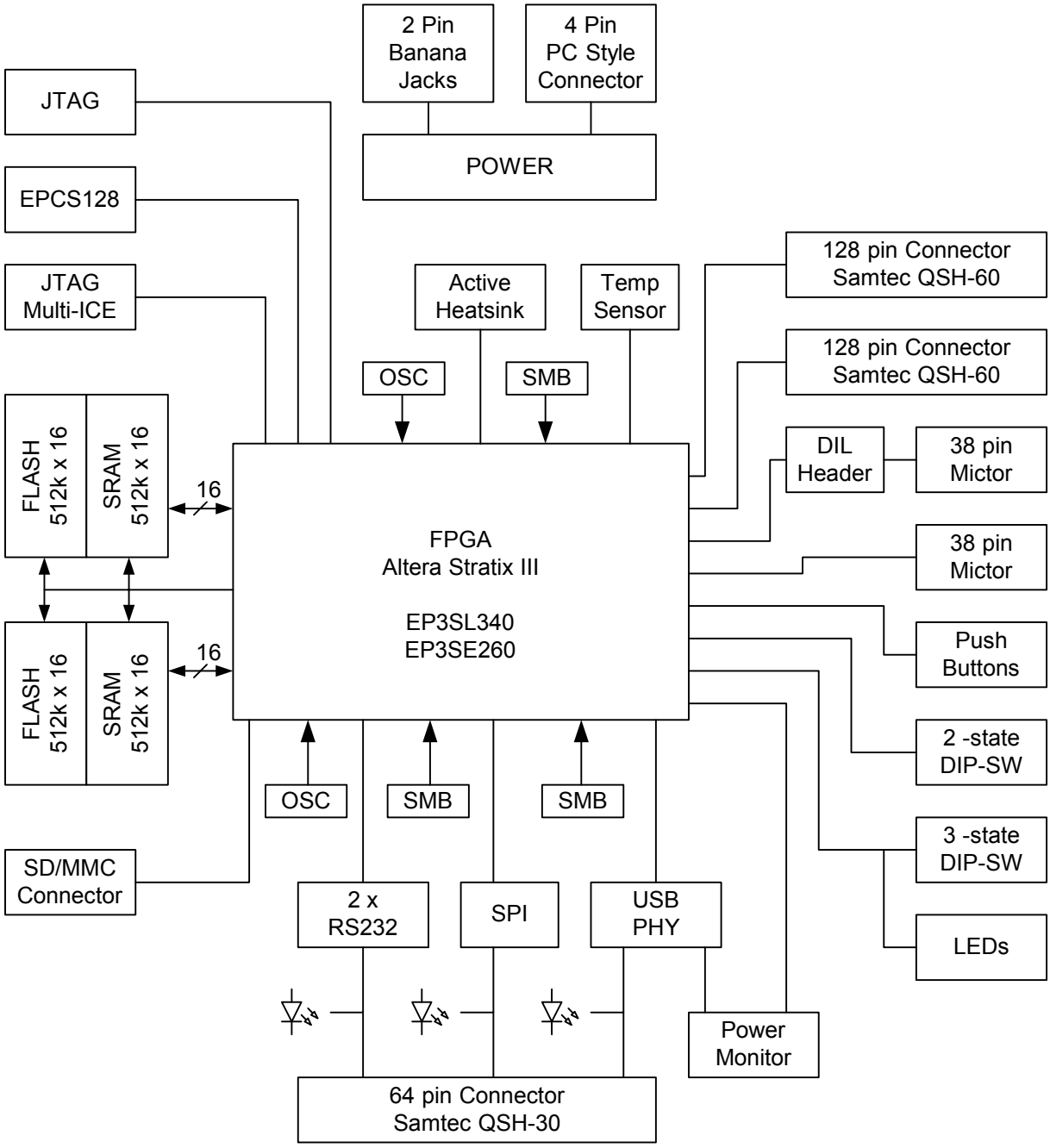
The development board must be stored between -40°C and 85°C. The recommended operating temperature is between 0°C and 70°C. Please contact El Camino for availability information on DIGILAB SX IIIs that support the industrial temperature range of -40°C to 85°C.

The board can be damaged without proper anti-static handling.
Anti-static precautions should be taken before handling the board.

Functional Description

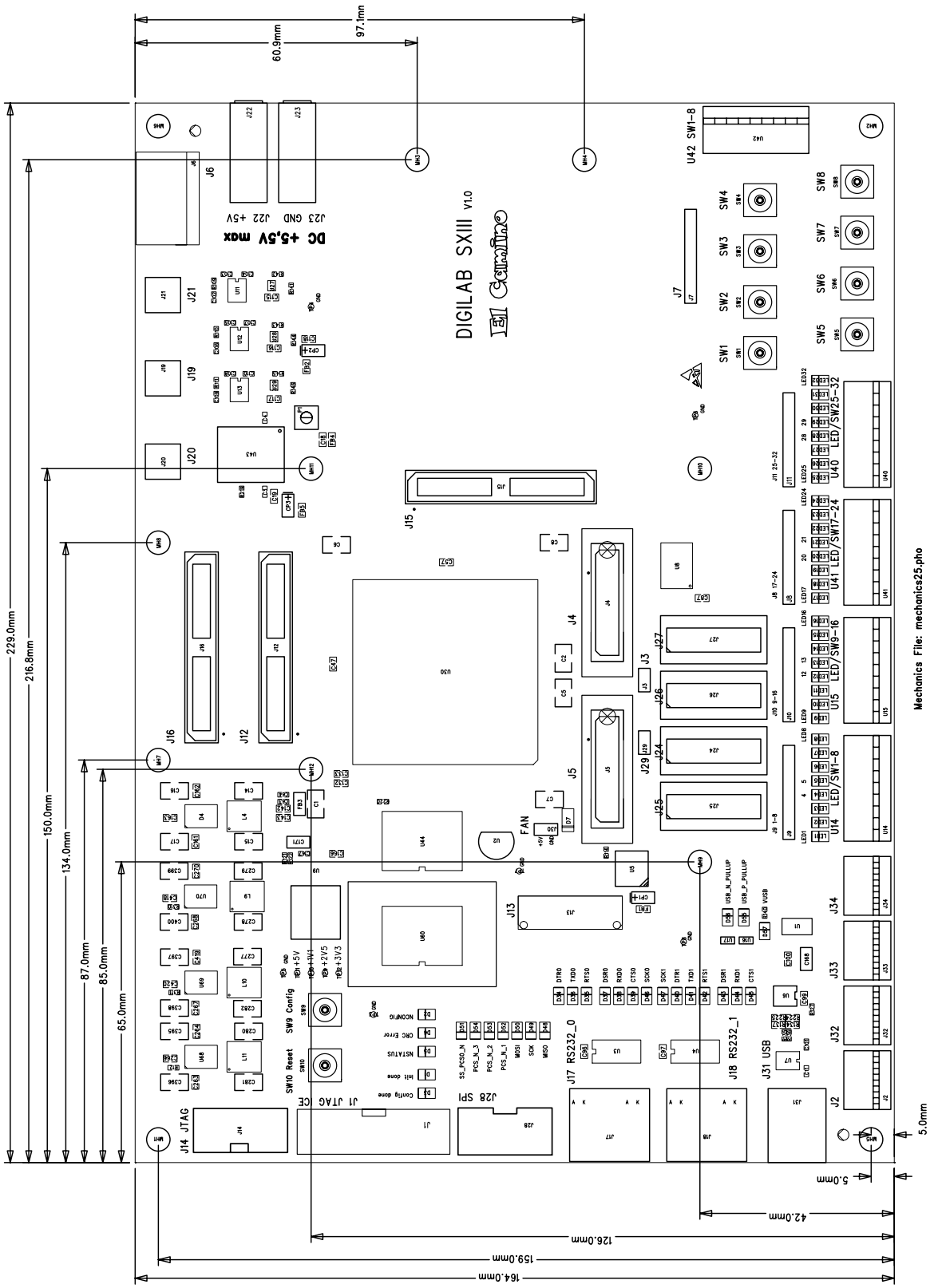
This section describes the elements of the DIGILAB SX III prototyping board. Figure 1 shows a block diagram of the board.

Figure 1: DIGILAB SX III Block Diagram



The DIGILAB SX III is a general purpose prototyping platform. Figure 2 shows the basic mechanical setup of the DIGILAB SX III. The measurements can be used to develop and manufacture custom adapter boards. Contact El Camino if you require further details on the mechanical dimensions of the board.

Figure 2: DIGILAB SX III Mechanical Setup - Top View



All measurements are in mm.

Stratix III Device

The DIGILAB SX III board can be equipped with any Stratix III device in a 1517 pin FineLine BGA package with 960 IOs. Devices currently supported in this package are the EP3SL340 and the EP3SE260. Furthermore it is possible to select any speed grade. Pricing and availability of the board will depend on the Stratix III device chosen.

Disable Unused Resources

When implementing custom user designs it is important to disable unused resources on the DIGILAB SX III, so that there are no bus contentions e.g. on the data bus connected to SRAM and FLASH.

In order to avoid contentions on the various switch and push button inputs it is recommended to either use the design template that is provided with the board or reserve all unused pins „As input tri-stated with weak pull-up resistor“. The board may be damaged if this guideline is not followed.

The SRAM and FLASH devices have pull-up resistors on their active low select lines.

Table 1: Disable Unused Resources

Function	Signal	Stratix III Pin	Value
SRAM	SRAM_CE1	D22	’1’ or ’Z’
	SRAM_CE2	B22	’1’ or ’Z’
FLASH	FLASH_CE1_N	J22	’1’ or ’Z’
	FLASH_CE2_N	A31	’1’ or ’Z’

Power Supply

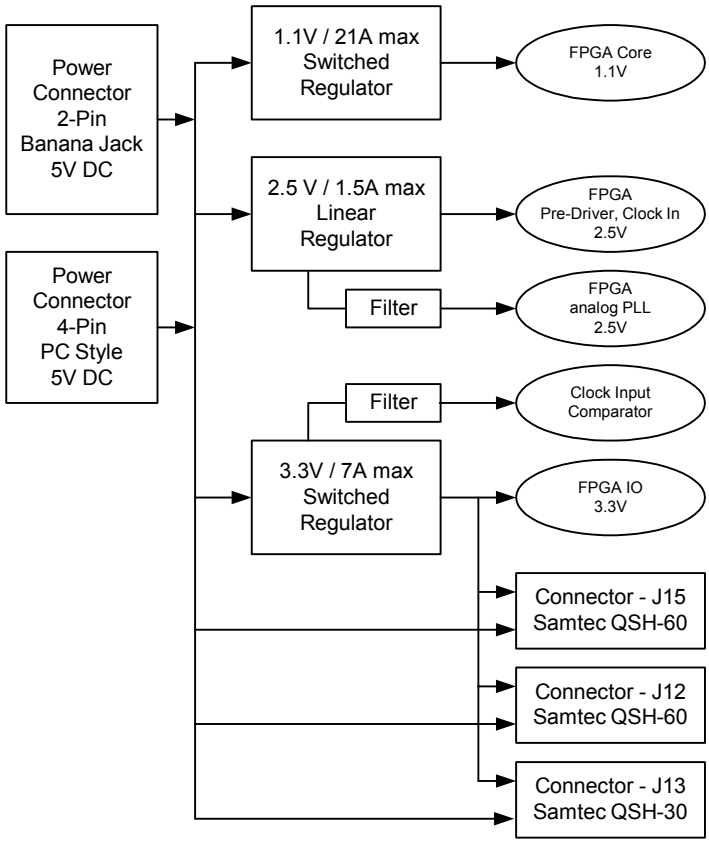
The DIGILAB SX III is meant to be used in a lab environment. It requires a 5V DC input and offers to optional power connectors. Power can be supplied through two banana jacks or a standard four pin PC style connector.

Table 2: Power Supply Options

Option	Voltage	Connector	Description
Banana Jacks	5V DC	J22 - +5V J23 - GND	For use with a Lab power supply
4-Pin PC Style Connector	5V DC	J6	For use with a standard PC power supply

The DC input current when unconfigured and during configuration is a approximately *TBD* mA at 5V DC. The input current while the maintenance design is running and during self-test is approximately *TBD* mA.

Figure 3: DIGILAB SX III Power Supply



Thermal considerations

The total power consumption can vary significantly, depending on the implemented design and the clock frequencies. Refer to information from Altera for details on Stratix III power consumption. We strongly recommend to do a power analysis and/or monitor the Stratix III case temperature during operation.

Depending on the design implemented and the total power consumption, active cooling may be necessary. A 5V DC cooling fan is connected to J30. The fan can be controlled from within the FPGA by driving the PWM_FAN signal. Furthermore, the board is equipped with an ac-

tive temperature sensor that is mounted with a thermal adhesive to the board in close proximity to the FPGA. The board comes with an encrypted IP function, that reads the temperature once per second and controls the cooling fan. The IP function has the following IO ports and parameters and can be instantiated in a user design. Alternatively the fan control signal PWM_FAN can be left floating or driven high to permanently turn on the fan. During configuration the fan will be on, which gives some feedback on the functionality of the fan at each power or configuration cycle.

Figure 4: Fan Control

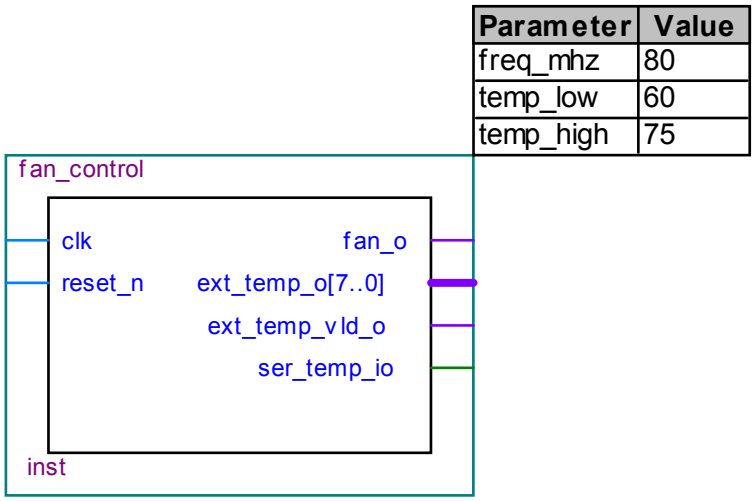


Table 3: Fan Control Ports and Parameters

	Name	Direction	Function
Parameter	freq_mhz	in	Specifies the clock frequency in MHz. Used to calculate timing for accessing the temperature sensor
	temp_low	in	Temperature in degree Celsius at which the fan will start to receive PWM pulses
	temp_high	in	Temperature in degree Celsius at which the fan will be fully turned on
Ports	clk	in	Clock input
	reset_n	in	Low active reset input, de-assertion should be synchronized to clk externally
	fan_o	out	Control signal for the fan; should be connected to PWM_FAN on the board
	ext_temp_o[7..0]	out	Actual temperature in degree Celsius (signed), valid while ext_temp_vld_o is high
	ext_temp_vld_o	out	High while ext_temp_o is valid
	ser_temp_io	inout	Interface to the temperature sensor, connect to SER_TEMP_DATA_PCB through a bi-directional pin

SRAM

U31 and U32 are two 1 MByte (512k x 16) asynchronous SRAM devices. They are connected to the Stratix III device so that they can be used by any custom logic in the FPGA or by a Nios II processor as general-purpose memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The SRAM shares a common bus with the on-board FLASH devices.

A data sheet for the SSRAM devices can be found at:
URL: http://www.issi.com
Type: IS61LV51216

The pinout can be found in the following table or it can be extracted from the netlist, that comes with the board.

CFI Flash Memory

U60 and U44 are two 1 MByte (512k x 16) CFI FLASH memory devices that can be used as a general purpose, non-volatile storage. They are connected to the Stratix III device so that they can be used by any custom logic in the FPGA or by a Nios II processor as general-purpose, non-volatile memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The FLASH devices share a common bus with the on-board SRAM devices.

A data sheet for the Flash memory devices can be found at:
URL: http://www.sst.com
Type: SST39LF800

The pinout can be found in the following table or it can be extracted from the netlist, that comes with the board.

Table 4: Memory Signals - SRAM U31/U32 and FLASH U60/U44

Signal	Stratix III U30	SRAM	FLASH	Signal	Stratix III U30	SRAM	FLASH
DQ_0	B34	U31	U60	A0	M26	both	both
DQ_1	A34	U31	U60	A1	N26	both	both
DQ_2	A35	U31	U60	A2	G18	both	both
DQ_3	B36	U31	U60	A3	K29	both	both
DQ_4	A36	U31	U60	A4	G29	both	both
DQ_5	B37	U31	U60	A5	J31	both	both
DQ_6	A37	U31	U60	A6	J30	both	both
DQ_7	A38	U31	U60	A7	F30	both	both
DQ_8	C35	U31	U60	A8	D31	both	both
DQ_9	C32	U31	U60	A9	D34	both	both
DQ_10	F32	U31	U60	A10	E31	both	both
DQ_11	G32	U31	U60	A11	E33	both	both
DQ_12	E22	U31	U60	A12	E34	both	both
DQ_13	F21	U31	U60	A13	G31	both	both
DQ_14	F31	U31	U60	A14	H30	both	both
DQ_15	F33	U31	U60	A15	K28	both	both
DQ_16	A22	U32	U44	A16	G15	both	both
DQ_17	A23	U32	U44	A17	M27	both	both
DQ_18	B24	U32	U44	A18	L27	both	both
DQ_19	A24	U32	U44	A19	J27		both
DQ_20	A25	U32	U44	A20	K27		both
DQ_21	A32	U32	U44	SRAM_WE	D33	both	
DQ_22	B33	U32	U44	SRAM_OE	F22	both	
DQ_23	A33	U32	U44	SRAM_CE1	D22	U31	
DQ_24	C34	U32	U44	SRAM_LB1	M25	U31	
DQ_25	D35	U32	U44	SRAM_UB1	F23	U31	
DQ_26	C21	U32	U44	SRAM_CE2	B22	U32	
DQ_27	D24	U32	U44	SRAM_LB2	F20	U32	
DQ_28	E24	U32	U44	SRAM_UB2	D21	U32	
DQ_29	D23	U32	U44	FLASH_OE_N	A29		both
DQ_30	C23	U32	U44	FLASH_WE_N	M24		both
DQ_31	C22	U32	U44	FLASH_CE1_N	J22		U60
				FLASH_CE2_N	A31		U44

RS-232 Serial Interfaces

The DIGILAB SX III provides two independent bidirectional RS-232 serial I/O interfaces. The board contains the transceiver (U3, U4), however the logic controller (UART) must be implemented in the Stratix III device.

J17 and J18 are standard RJ45 connectors. These connectors can be used for communication with a host computer using an adapter cable to connected for example to a COM port. In addition, all RS-232 signals are available through J13, a Samtec QSH-30 connector, which allows to connect custom add-on or interface boards.

J17 and J18 can transmit all RS-232 signals. The Stratix III design may use only signals it needs, such as RXD and TXD. LEDs are connected to all RS232 signals, giving a visual indication, whether data is being transmitted or received. The following table shows the pin mapping between the Stratix III device and the RS232 signals.

A data sheet for the RS-232 transceiver can be found at:
URL: http://www.maxim-ic.com
Type: MAX3238

Table 5: RS-232 Interfaces

Interface	Function	Stratix III - U30		RJ45 Connector	Samtec Connectors J13
		Signal	Pin		
J17 RS232_0	DTR	USART_DTR_0	A6	J17 - 1, 2	22
	TXD	USART_TXD_0	A5	J17 - 5	8
	RTS	USART_RTS_0	A4	J17 - 7	20
	DSR	USART_DSR_0	A3	J17 - 3	30
	RXD	USART_RXD_0	B3	J17 - 6	6
	CTS	USART_CTS_0	B4	J17 - 8	18
	Enable	USART0_EN	B6	n/a	n/a
	n/a	USART_SCK_0	L16	n/a	10
J18 RS232_1	DTR	USART_DTR_1	F7	J18 - 1, 2	21
	TXD	USART_TXD_1	G7	J18 - 5	7
	RTS	USART_RTS_1	G8	J18 - 7	19
	DSR	USART_DSR_1	F8	J18 - 3	29
	RXD	USART_RXD_1	E7	J18 - 6	5
	CTS	USART_CTS_1	F6	J18 - 8	17
	Enable	USART1_EN	D4	n/a	n/a
	n/a	USART_SCK_1	A2	n/a	9

SPI Interface

The DIGILAB SX III provides an SPI interface through general purpose Stratix III I/O pins. Besides an ESD protection, there are no special buffers or level shifters implemented. In order to use the SPI interface, a logic controller for SPI must be implemented in the Stratix III device.

The SPI interface is available through J28, a standard dual row 2x5 header. In addition, all SPI signals are available through J13, a Samtec QSH-30 connector, which allows to connect custom add-on or interface boards.

LEDs are connected to all SPI signals, giving a visual indication, whenever data is being transmitted or received. The following table shows the pin mapping between the Stratix III device and the SPI signals.

Table 6: SPI Interface

Function	Stratix III - U30		J28 2x5 Header	Samtec Connectors J13
	Signal	Pin		
GND	n/a	n/a	1	n/a
GND	n/a	n/a	2	n/a
3.3V	n/a	n/a	3	n/a
SCK	SPI_SCK	C6	4	39
MISO	SPI_MISO	D11	5	32
MOSI	SPI_MOSI	J15	6	31
PCS_2	SPI_PCS_N_2	C15	7	42
PCS_3	SPI_PCS_N_3	A7	8	41
PCS_0	SPI_SS_PCS0_N	C13	9	40
PCS_1	SPI_PCS_N_1	B7	10	43

USB Interface

On the board, there is a USB transceiver that complies with USB 1.1, as well as a USB connector and a line protection device. USB 2.0 can be supported with a different, pin-compatible transceiver, that can be mounted on a request basis. The board provides the transceiver (U6), however the USB controller must be implemented in the Stratix III device.

J31 is a standard USB Type B connector. This connector can be used for communication with a host computer using a standard USB cable. In addition, the local signals of the USB transceiver are available through J13, a Samtec QSH-30 connector, which allows to connect custom add-on or interface boards.

LEDs are connected to the USB data signals, giving a visual indication whenever data is being transmitted. Furthermore, there is a LED (D57) that monitors the USB input voltage.

The USB interface has programmable pull-up resistors. They can be controlled through the signals USB_P_PULLUP (monitored through LED D55) and USB_N_PULLUP (monitored through LED D56) from within the FPGA.
Furthermore the presence of the USB 5V voltage can be monitored with LED D57 and the FPGA input VUSB.

A data sheet for the USB transceiver can be found at:
URL: http://www.fairchildsemi.com
Type: USB1T11A (for USB 2.0: USB1T20)

The following table shows the pin mapping between the Stratix III device and the USB signals.

Table 7: USB Interface

Function	Stratix III - U30		Samtec Connectors J13
	Signal	Pin	
VPO	USB_TXD	E16	53
VMO	USB_EOP	F17	55
OE_N	USB_TXOE_N	A13	54
SUSPND	USB_ON_N	A14	56
VP	USB_RXDP	B13	52
VM	USB_RXDM	F18	51
RCV	USB_RXD	D15	44
D+ Pull-Up	USB_P_PULLUP	A8	n/a
D- Pull-Up	USB_N_PULLUP	A10	n/a
VBUS Monitor	VUSB	D1	n/a

Multi-ICE JTAG Interface

The Multi-ICE JTAG connector allows the connection of a Multi-ICE interface unit to the board. The connection enables debugging of ARM processors implemented inside the Stratix III FPGA. All signals feature

ESD protection and are directly connected to standard Stratix III I/O pins. The signal mapping can be found in the following table:

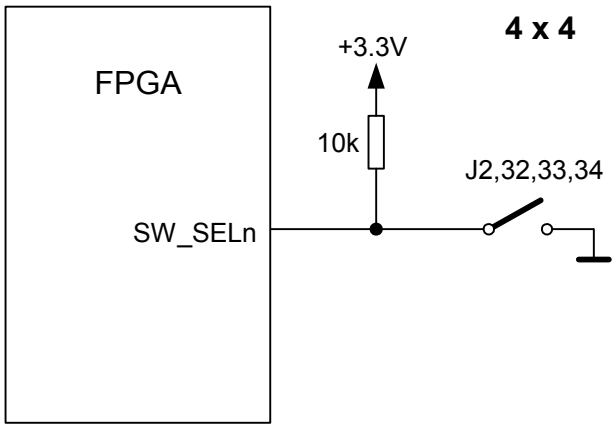
Table 8: Multi-ICE JTAG Connector

Signal	J1 Connector		Signal	Stratix III U30 Pin
	Pin	Pin		
3.3V	2	1	3.3V	n/a
GND	4	3	ICE_TRST_N	B16
GND	6	5	ICE_TDI	A17
GND	8	7	ICE_TMS	C18
GND	10	9	ICE_TCK	C17
GND	12	11	ICE_RTCK	D18
GND	14	13	ICE_TDO	A18
GND	16	15	ICE_SRST_N	B18
GND	18	17	ICE_DBGRQ	E18
GND	20	19	ICE_DBGACK	E19

DIP Switches (two-state)

The DIGILAB SX III has 16 two-state DIP switches. They switch between GND (when on) and a 10k Ohm pull-up resistor (when off). The following diagram shows the functionality of the two-state switches.

Figure 5: Two-state DIP switches



The signal mapping for the 2-state DIP switches can be found in the folowing table:

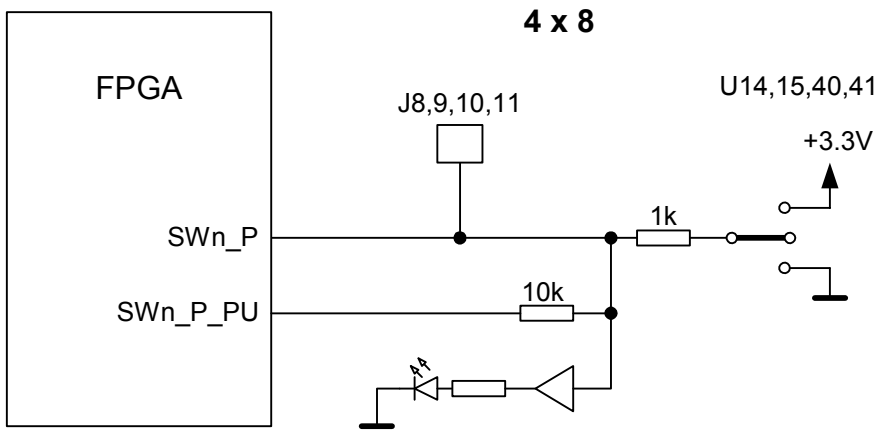
Table 9: DIP Switches (two-state)

DIP Switch		Signal	Stratix III - U30 Pin
J2	1	SW_SEL1	P10
	2	SW_SEL2	P9
	3	SW_SEL3	G2
	4	SW_SEL4	F2
J32	1	SW_SEL5	N11
	2	SW_SEL6	P12
	3	SW_SEL7	H4
	4	SW_SEL8	H3
J33	1	SW_SEL9	N10
	2	SW_SEL10	N9
	3	SW_SEL11	J5
	4	SW_SEL12	J4
J34	1	SW_SEL13	M9
	2	SW_SEL14	M8
	3	SW_SEL15	G4
	4	SW_SEL16	G3

DIP Switches (three-state) and User LEDs

The DIGILAB SX III has a total of 32 three-state DIP switches in four groups of eight.

Figure 6: Three-state DIP switches



The signals driven by these switches are also connected to programmable pull-up/down resistors, as well as LEDs through drivers. The FPGA signal SWn_P can be used as an input, driven by the switch and pulled high or low through SWn_P_PU. Alternatively, when the switch is not used, the signal SWn_P can be used as output driven by the FPGA and controlling the LED. The LEDs will show the current status of the line.

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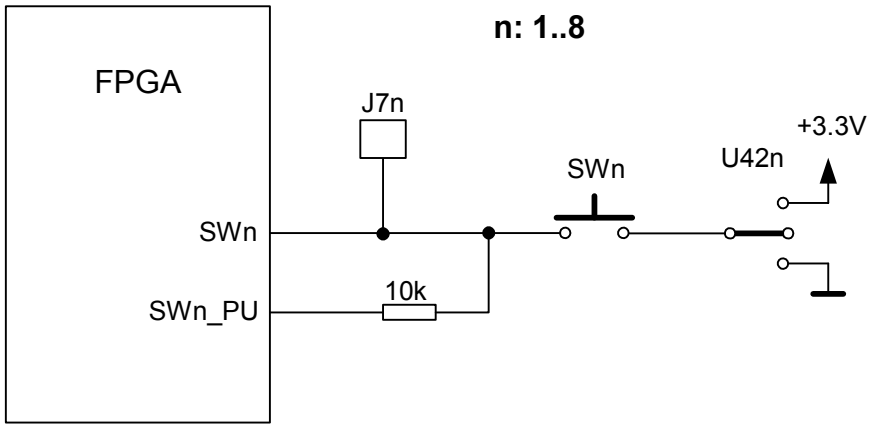
Table 10: Three-state DIP switches and LEDs

Switch		LED	Signal		Pull-Up/Down Resisotr	
			Name	Stratix III U30 - Pin	Name	Stratix III U30 - Pin
U14	1	LED1	SW1_P	AA7	SW1_P_PU	AB7
	2	LED2	SW2_P	AB5	SW2_P_PU	AB9
	3	LED3	SW3_P	AB11	SW3_P_PU	AB12
	4	LED4	SW4_P	AC6	SW4_P_PU	AC7
	5	LED5	SW5_P	AD10	SW5_P_PU	AD11
	6	LED6	SW6_P	AD9	SW6_P_PU	AD12
	7	LED7	SW7_P	AD7	SW7_P_PU	AD8
	8	LED8	SW8_P	AD6	SW8_P_PU	AE6
U15	1	LED9	SW9_P	AC9	SW9_P_PU	AC10
	2	LED10	SW10_P	AE3	SW10_P_PU	AF6
	3	LED11	SW11_P	AF7	SW11_P_PU	AG5
	4	LED12	SW12_P	AG6	SW12_P_PU	AE11
	5	LED13	SW13_P	AE9	SW13_P_PU	AF9
	6	LED14	SW14_P	AE10	SW14_P_PU	AG7
	7	LED15	SW15_P	AG8	SW15_P_PU	AK6
	8	LED16	SW16_P	AL3	SW16_P_PU	AL4
U41	1	LED17	SW17_P	AM3	SW17_P_PU	AM4
	2	LED18	SW18_P	AN3	SW18_P_PU	AN2
	3	LED19	SW19_P	AN4	SW19_P_PU	AN5
	4	LED20	SW20_P	AM6	SW20_P_PU	AH8
	5	LED21	SW21_P	AH6	SW21_P_PU	AG9
	6	LED22	SW22_P	AH7	SW22_P_PU	AM1
	7	LED23	SW23_P	AN1	SW23_P_PU	AL6
	8	LED24	SW24_P	AL5	SW24_P_PU	AG11
U40	1	LED25	SW25_P	AG10	SW25_P_PU	AH12
	2	LED26	SW26_P	AH11	SW26_P_PU	AL2
	3	LED27	SW27_P	AK3	SW27_P_PU	AF12
	4	LED28	SW28_P	AP1	SW28_P_PU	AG13
	5	LED29	SW29_P	AR3	SW29_P_PU	AP2
	6	LED30	SW30_P	AT2	SW30_P_PU	AR4
	7	LED31	SW31_P	AT1	SW31_P_PU	AT3
	8	LED32	SW32_P	AR1	SW32_P_PU	AK5

Push Buttons

The DIGILAB SX III features 8 user configurable push buttons. Through an 8-bit three-state DIP switch, the push buttons can be set to be active low, active high or disabled. Furthermore there are programmable pull-up/down resistors for every push button signal. The following diagram shows the functionality of a single push button.

Figure 7: Push Buttons



SD/MMC Connector

The DIGILAB SX III features an SD (Secure Digital)/MultiMediaCard (MMC) card connector (U61). This connector can be used to insert standard SD/MMC cards. The SD/MultiMediaCard card is a universal low cost data storage and communication media. It was designed to cover a wide area of applications, such as electronic toys, organizers, PDAs, cameras, smart phones, digital recorders, MP3 players, etc. The SD/MultiMediaCard card communication is based on an advanced 7-pin serial bus. All relevant SD/MMC signals are connected directly to the Stratix III device. On the DIGILAB SX III, SD/Multi Media cards may be used as a flexible, non-volatile and mobile storage media. It is up to the user to create an interface between the SD/MMC card and e.g. a NIOS II or custom logic. Contact El Camino for information on availability of ready to use SD/MMC interfaces, NIOS II library functions and drivers.

Table 11: SD/MMC Connector

SD Card Function		Connector U61 Pin	Stratix III U30	
SD Mode	SPI Mode		Signal	Pin
CD/DAT3	CS	1	MMC_RSV	AU25
CMD	DI	2	MMC_CMD	AU22
CLK	SCLK	5	MMC_CLK	AU30
DAT0	DO	7	MMC_DAT	AP25
DAT1		8	MMC_DAT2	AN22
DAT2		9	MMC9	AU26
WRITE_PROT_FRONT		12	MMC_WP1	AT28
CARD_DETECT		13	MMC_CDET	AU27

Debug Connectors

The DIGILAB SX III has various, different connectors that can be used to connect debugging logic to the board.

There are two 38 pin AMP/Tyco Matched Impedance Connectors (MICTOR) on the board. More information about these connectors can be found at:
URL: www.tycoelectronics.com
Type: 2-5767004-2

On each of these connectors, there are 32 standard Stratix III user IOs in addition to two PLL clock outputs/user IOs .
The signals of MICTOR connector J4 are routed directly to the FPGA and are therefor optimized for high speed. The signals of J5 are also available through standard dual row .100 inch headers (IOs on J24,25,26,27 and clocks on J3/J29) for easy access to individual signals.

The following tables lists the signal names and pin numbers for these connectors.

Table 12: MICTOR connector J5

Header		Stratix III U30 - Pin	Signal	J5		Signal	Stratix III U30 - Pin	Header	
Con.	Pin			Pin	Pin			Pin	Con.
N/A	N/A	N/A	GND	1	38	GND	N/A	N/A	N/A
N/A	N/A	N/A	GND	2	37	GND	N/A	N/A	N/A
J3	1	H21	LA_CLK0	3	36	LA_CLK1	L18	1	J29
J27	1	V1	LA_A3_7	4	35	LA_A1_7	V4	1	J24
	3	V2	LA_A3_6	5	34	LA_A1_6	V3	3	
	5	U1	LA_A3_5	6	33	LA_A1_5	U4	5	
	7	T1	LA_A3_4	7	32	LA_A1_4	U3	7	
	9	T2	LA_A3_3	8	31	LA_A1_3	T5	9	
	11	R1	LA_A3_2	9	30	LA_A1_2	T4	11	
	13	R2	LA_A3_1	10	29	LA_A1_1	R4	13	
	15	P1	LA_A3_0	11	28	LA_A1_0	R3	15	
J26	1	N1	LA_A2_7	12	27	LA_A0_7	P4	1	J25
	3	N2	LA_A2_6	13	26	LA_A0_6	P3	3	
	5	M1	LA_A2_5	14	25	LA_A0_5	N4	5	
	7	M2	LA_A2_4	15	24	LA_A0_4	M3	7	
	9	L1	LA_A2_3	16	23	LA_A0_3	M4	9	
	11	K1	LA_A2_2	17	22	LA_A0_2	L4	11	
	13	K2	LA_A2_1	18	21	LA_A0_1	L3	13	
	15	J1	LA_A2_0	19	20	LA_A0_0	K4	15	

Table 13: High-Speed MICTOR connector J4

Stratix III U30 - Pin	Signal	J5		Signal	Stratix III U30 - Pin
		Pin	Pin		
N/A	GND	1	38	GND	N/A
N/A	GND	2	37	GND	N/A
AH21	LA_CLK3	3	36	LA_Q1_CLK	AM19
AL1	LA_C1_7	4	35	LA_C3_7	AJ4
AK2	LA_C1_6	5	34	LA_C3_6	AJ3
AK1	LA_C1_5	6	33	LA_C3_5	AH5
AJ1	LA_C1_4	7	32	LA_C3_4	AH4
AH2	LA_C1_3	8	31	LA_C3_3	AG4
AH1	LA_C1_2	9	30	LA_C3_2	AG3
AG2	LA_C1_1	10	29	LA_C3_1	AF4
AG1	LA_C1_0	11	28	LA_C3_0	AF3
AF1	LA_C0_7	12	27	LA_C2_7	AE5
AE2	LA_C0_6	13	26	LA_C2_6	AE4
AE1	LA_C0_5	14	25	LA_C2_5	AD5
AD2	LA_C0_4	15	24	LA_C2_4	AD4
AD1	LA_C0_3	16	23	LA_C2_3	AC4
AC1	LA_C0_2	17	22	LA_C2_2	AC3
AB2	LA_C0_1	18	21	LA_C2_1	AB4
AB1	LA_C0_0	19	20	LA_C2_0	AB3

Expansion Connectors

The DIGILAB SX III has various connectors that can be used to connect user logic or custom adapter boards.

There are three 120 pin (J12, J15, J16) as well as one 60 pin (J13) Samtec QSH Hi-Speed connectors on the board.
More information about the connectors can be found on the Samtec website at:
URL: www.samtec.com
Type: QSH-060-.../QSH-030-...

Details on the pinout of these connectors can be found in the schematics or in the netlist, that is provided with the DIGILAB SX III.

Clocking

The DIGILAB SX III development board includes an 80 MHz oscillator, as well as an optional 20 MHz temperature compensated oscillator that drive the Stratix III FPGA. In addition there are three SMA clock inputs, feeding comparators, driving into clock buffers. The clock buffers are driving the FPGA and various expansion connectors. The signal length between A, B and C clocks are closely matched in order to provide minimal skew between the individual, external clocks.

The Stratix III FPGA contains multiple phase locked loops (PLLs) and global clock networks for clock management. Stratix III PLLs offer clock multiplication and division, phase shifting, programmable duty cycle, external clock outputs and more, allowing system-level clock management and skew control on the DIGILAB SX III.
The following diagram shows all clock inputs and outputs and how they are connected to the individual PLLs and connectors.

All unused, dual purpose clock inputs are connected to GND on the board. It is important that these pins are either reserved as inputs or reserved as IOs driving ground in the user design.

Figure 8: Clocking Circuitry

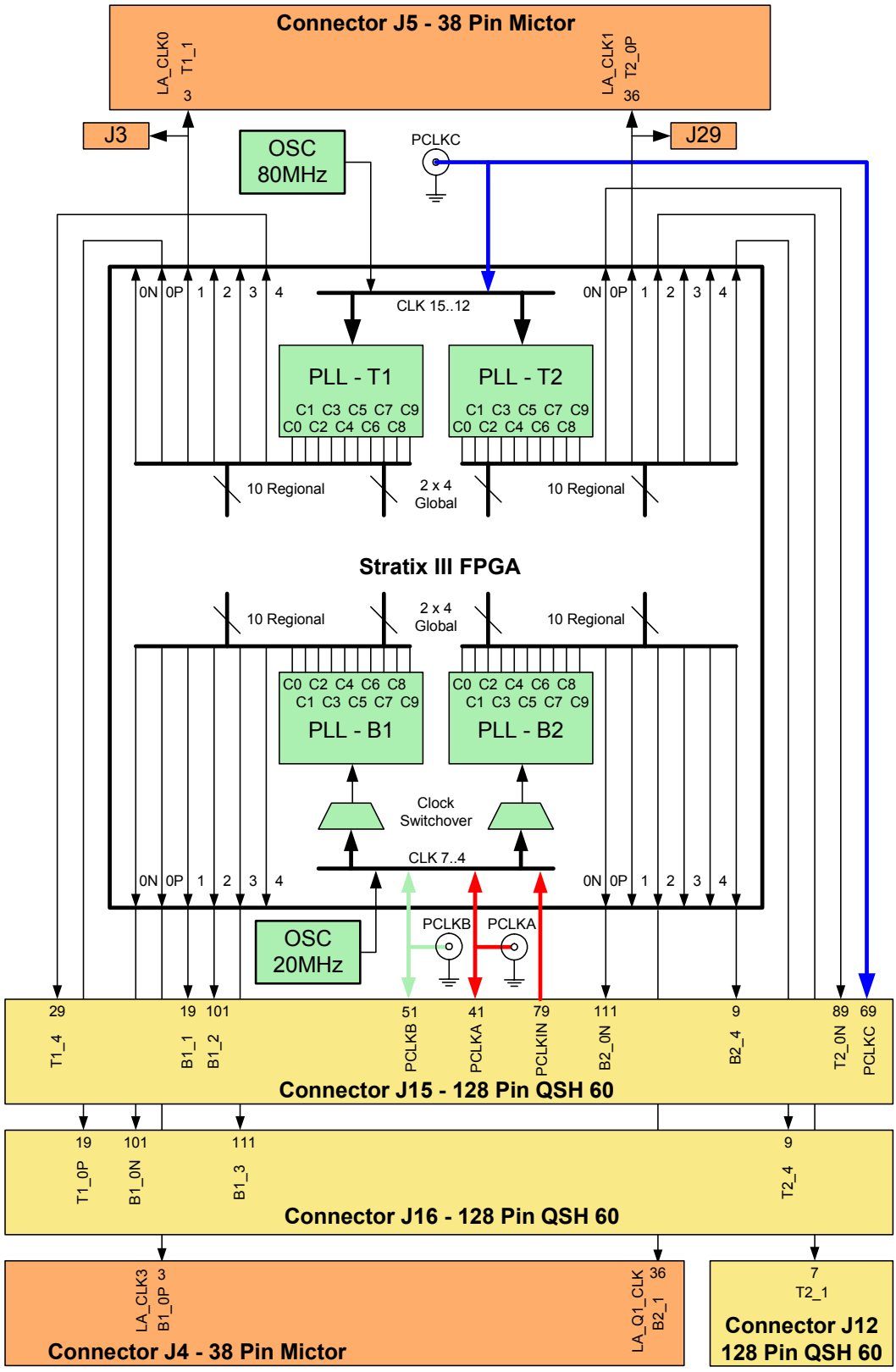


Table 14: Clock Signals

Signal	Dir. at FPGA	Board Connection	Stratix III Clock Signal	PLL	Stratix III Pin
80MHz	IN	oscillator - U5	CLK13P	T1,T2	B19
100MHz (100/20 MHz, optional)	IN	oscillator - U43	CLK6P	B1,B2	AT20
PCLKA_FPGA	IN	J21(SMA) J15-41	CLK5P	B1,B2	AV21
PCLKB_FPGA	IN	J19(SMA) J15-51	CLK4P	B1,B2	AT21
PCLKC_FPGA	IN	J20(SMA) J15-69	CLK12P	T1,T2	D19
PCLKIN	IN	J15-79	CLK7P	B1,B2	AV19
PLL_B1_CLKOUT0N	OUT	J16-101	0N	B1	AH22
PLL_B1_CLKOUT0P, LA_CLK3	OUT	J4-3	0P	B1	AH21
PLL_B1_CLKOUT3	OUT	J16-111	3	B1	AJ22
PLL_B1_CLKOUT2	OUT	J15-101	2	B1	AN21
PLL_B1_CLKOUT1	OUT	J15-19	1	B1	AM21
PLL_B2_CLOUT0N	OUT	J15-111	0N	B2	AH20
PLL_B2_CLKOUT4	OUT	J15-9	4	B2	AJ19
PLL_B2_CLKOUT1, LA_Q1_CLK	OUT	J4-36	1	B2	AM19
PLL_T2_CLKOUT0N	OUT	J15-89	0N	T2	K18
PLL_T2_CLKOUT0P, LA_CLK1	OUT	J5-36, J29-1	0P	T2	L18
PLL_T2_CLKOUT4	OUT	J16-9	4	T2	M19
PLL_T2_CLKOUT1	OUT	J12-7	1	T2	H19
PLL_T1_CLKOUT0P	OUT	J16-19	0P	T1	M21
PLL_T1_CLKOUT4	OUT	J15-29	4	T1	K22
PLL_T1_CLKOUT1, LA_CLK0	OUT	J5-3, J3-1	1	T1	H21

Configuration

The DIGILAB SX III uses an Altera EPCS128 serial configuration device for non-volatile configuration data storage. The FPGA is setup for Fast Active Serial configuration mode (Fast AS, 40 MHz). Upon power-up the DIGILAB SX III will start configuration from address 0x0 of the serial configuration device. A configuration cycle can also be triggered by pushing SW9 (marked as „SW9 Config“) which pulls the nConfig input of the FPGA low.
In addition, the FPGA can be programmed through the JTAG interface.

JTAG Connector

J14 is a 10-pin JTAG interface connector compatible with current Altera ByteBlaster, USB-Blaster and Ethernet-Blaster download cables. The JTAG connection can be used for any of the following purposes:

- Quartus II software can configure the Stratix III device (U30) with a new bitstream (such as .sof) file.
- Quartus II can re-program the serial configuration device EPCS with a JTAG indirect configuration file (.jic)
- The following Altera JTAG accessible functions can be used:
  - SignalTap II Logic Analyzer
  - In-System Memory Content Editor
  - Logic Analyzer Interface Editor
  - In-System Sources and Probes
  - NIOS II Debugging Interface

The JTAG programming interface is not available if the Stratix III has been protected by programming a non-volatile security key.

The JTAG connection is most commonly used to download user configuration files (such as .sof) to the Stratix device during logic development and debugging.

Notes:

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Germany
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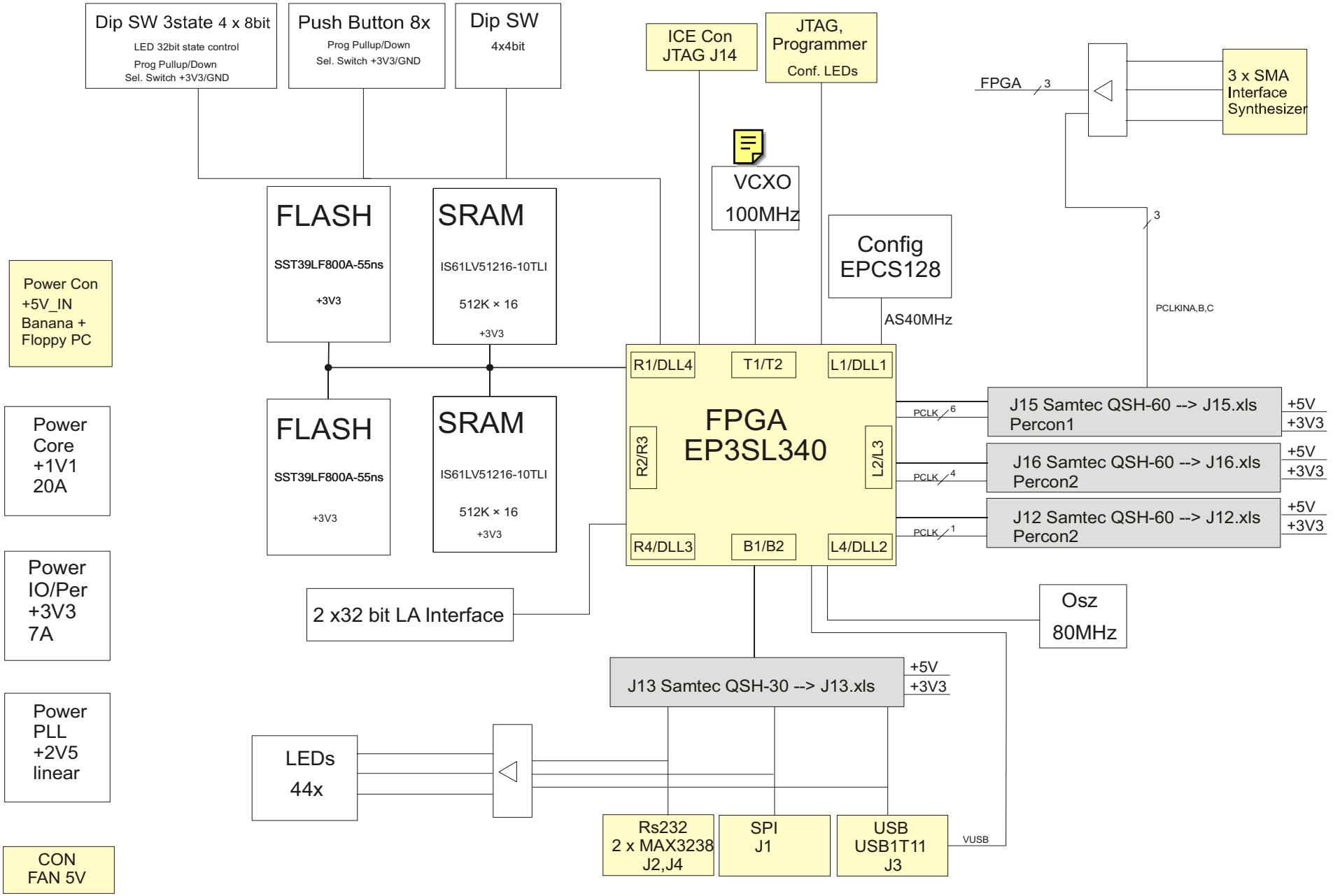
Telefax +49-8751-842876
E-mail: info@elca.de
http://www.elcamino.de

DIGILAB SX III V1.0



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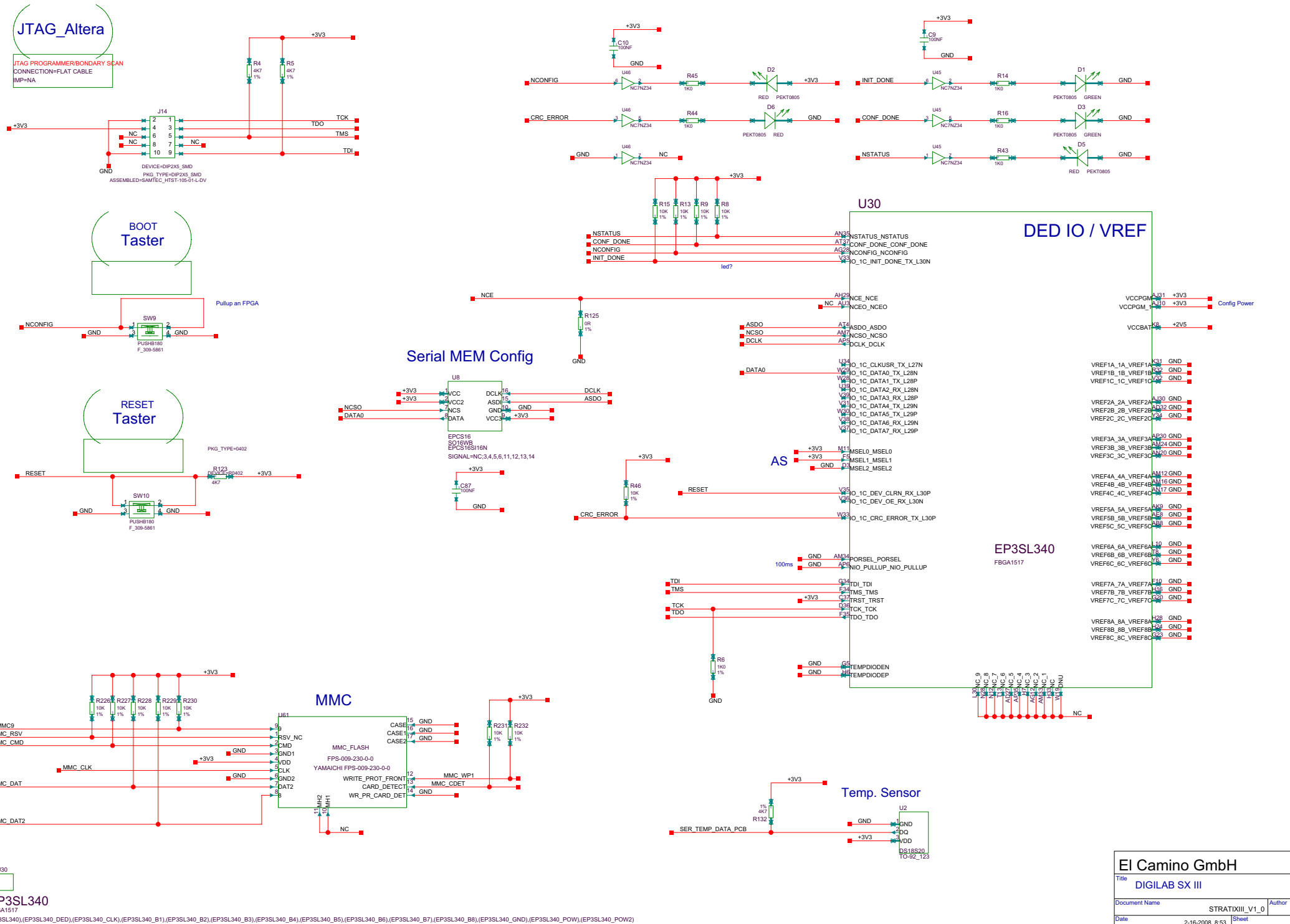
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Taster
Pullup an FPGA
SW9
PUSHB180
F_309-5861
RESET
Taster
PKG_TYPE=0402
SW10
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F_309-5861
Serial MEM Config
U8
EPCS16
SO16WB
EPCS16SI16N
SIGNAL=NC;3,4,5,6,11,12,13,14
U30
DED IO / VREF
EP3SL340
FBGA1517
AS
100ms
led?
Config Power
MMC
MMC_FLASH
FPS-009-230-0-0
YAMAICHI FPS-009-230-0-0
Temp. Sensor
DS18S20
TO-92_123
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2
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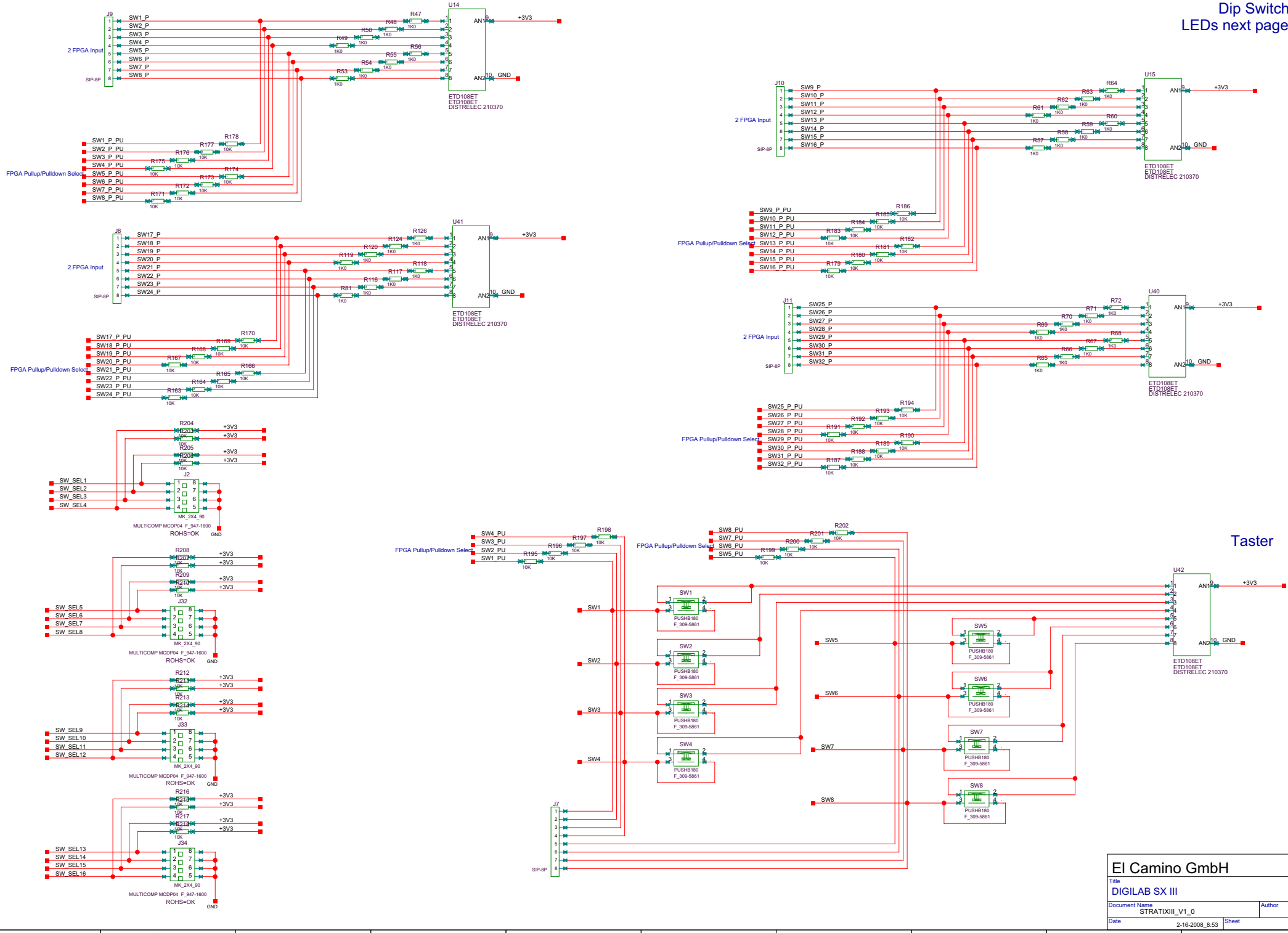
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FPGA Pullup/Pulldown Select
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ETD108ET
DISTRELEC 210370
Taster
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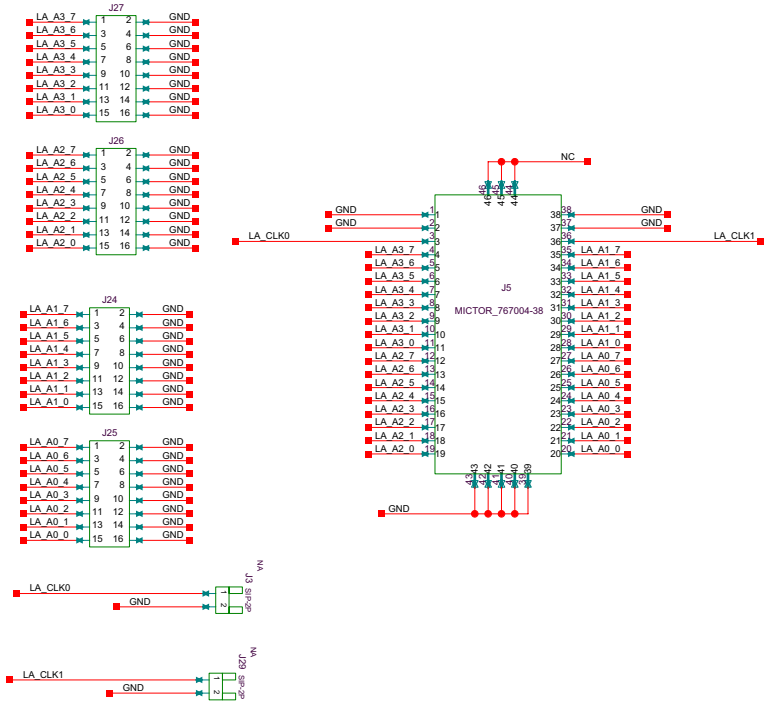
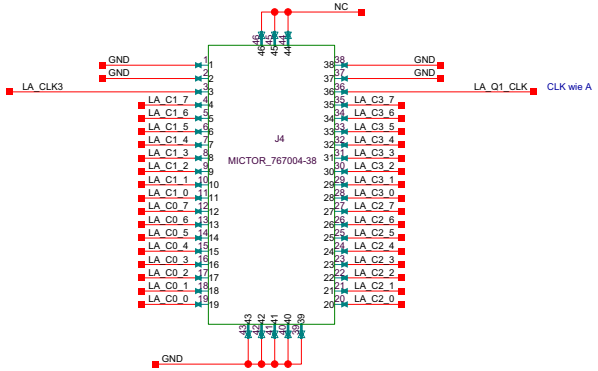
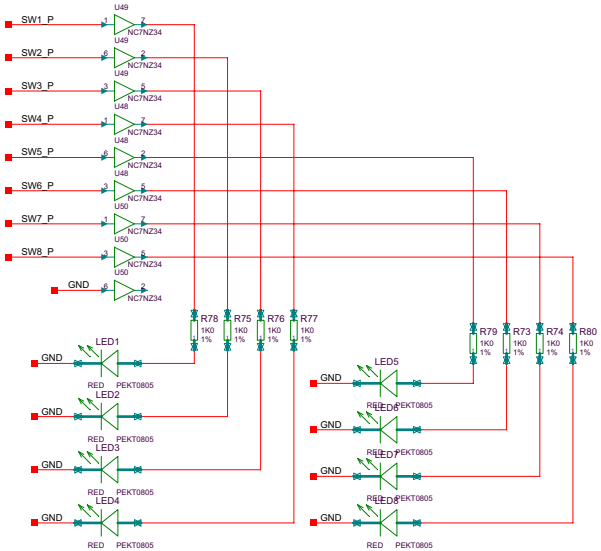
LEDs

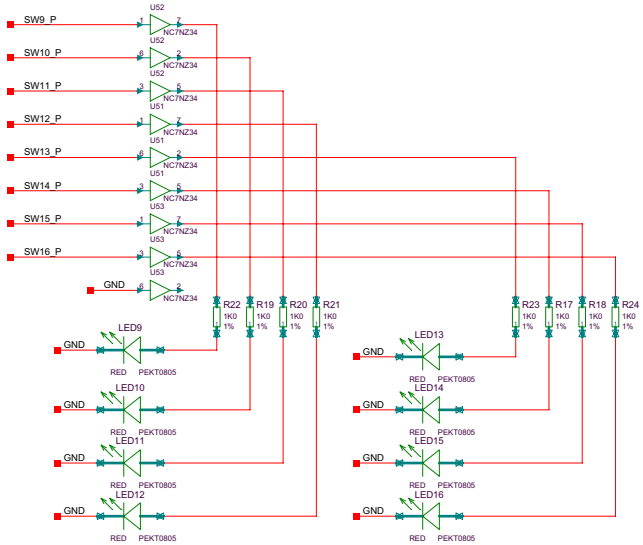
Gen. IO / LA Interface

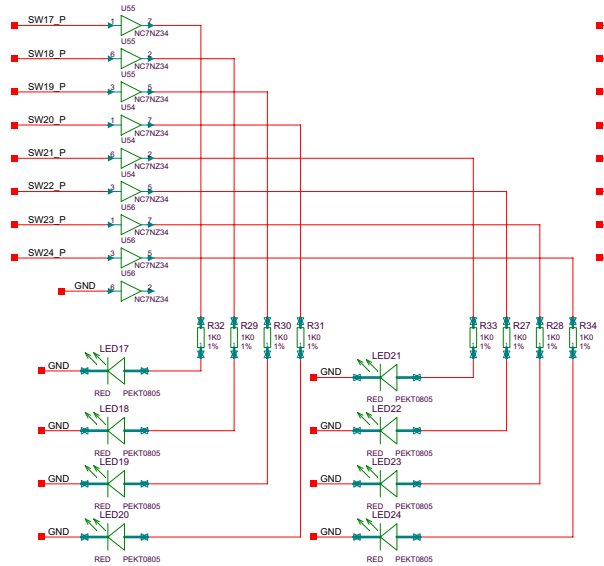


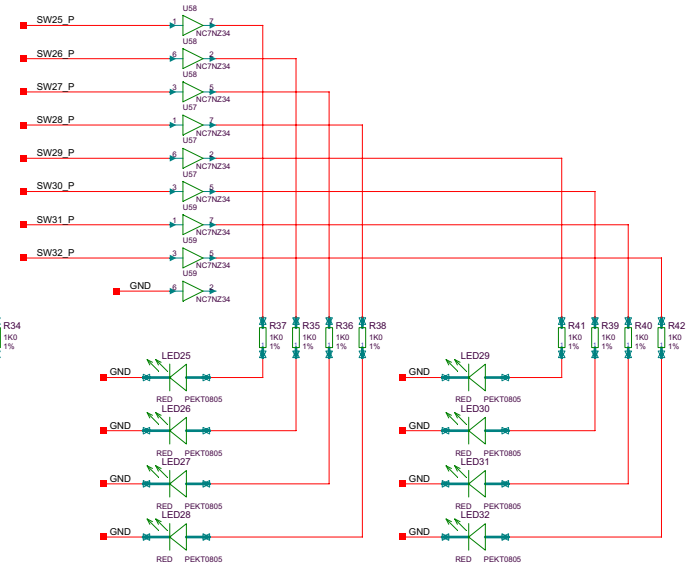
High Speed Gen. IO / LA Interface











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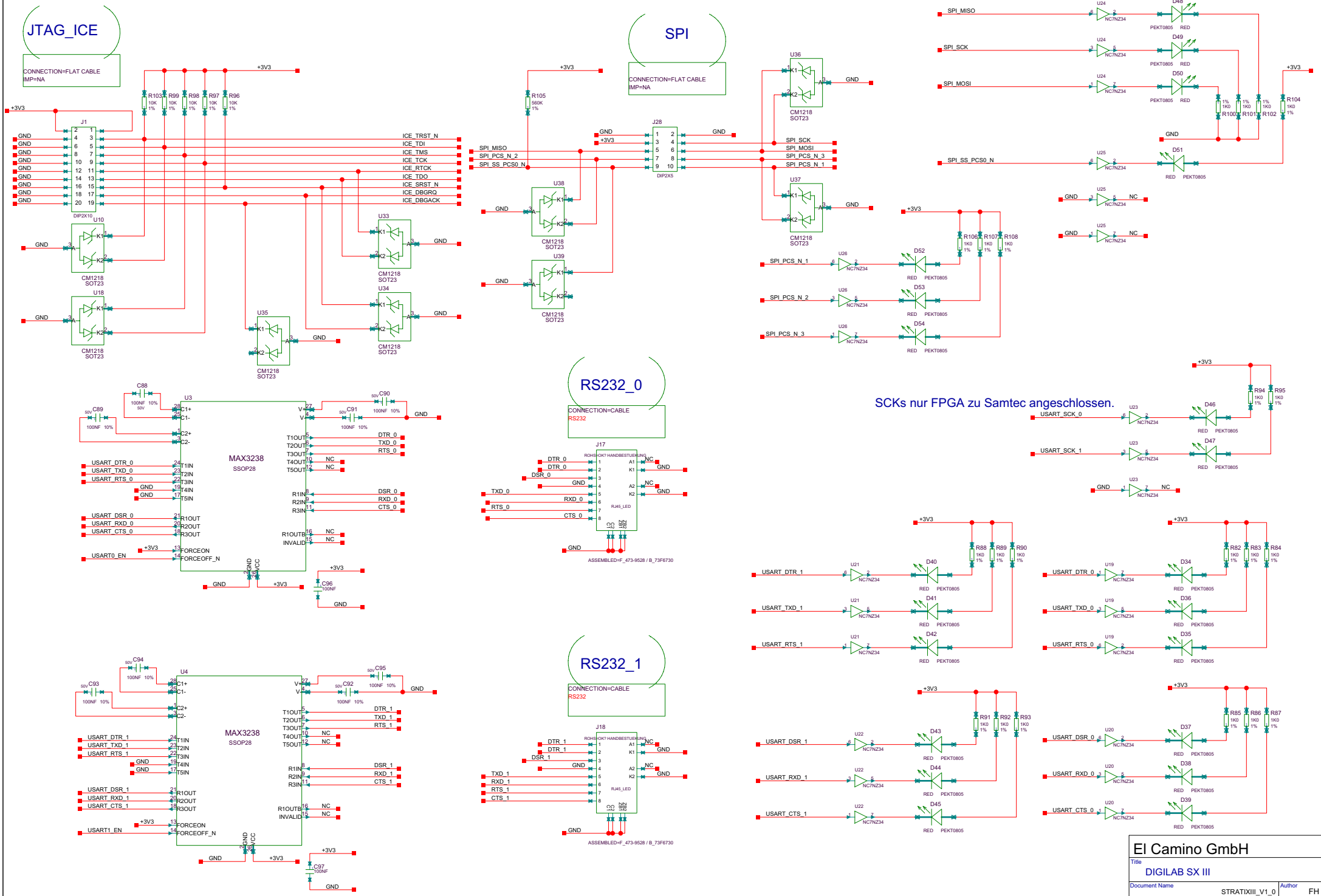
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IMP=NA
SPI
CONNECTION=FLAT CABLE
IMP=NA
RS232_0
CONNECTION=CABLE
RS232
RS232_1
CONNECTION=CABLE
RS232
SCKs nur FPGA zu Samtec angeschlossen.
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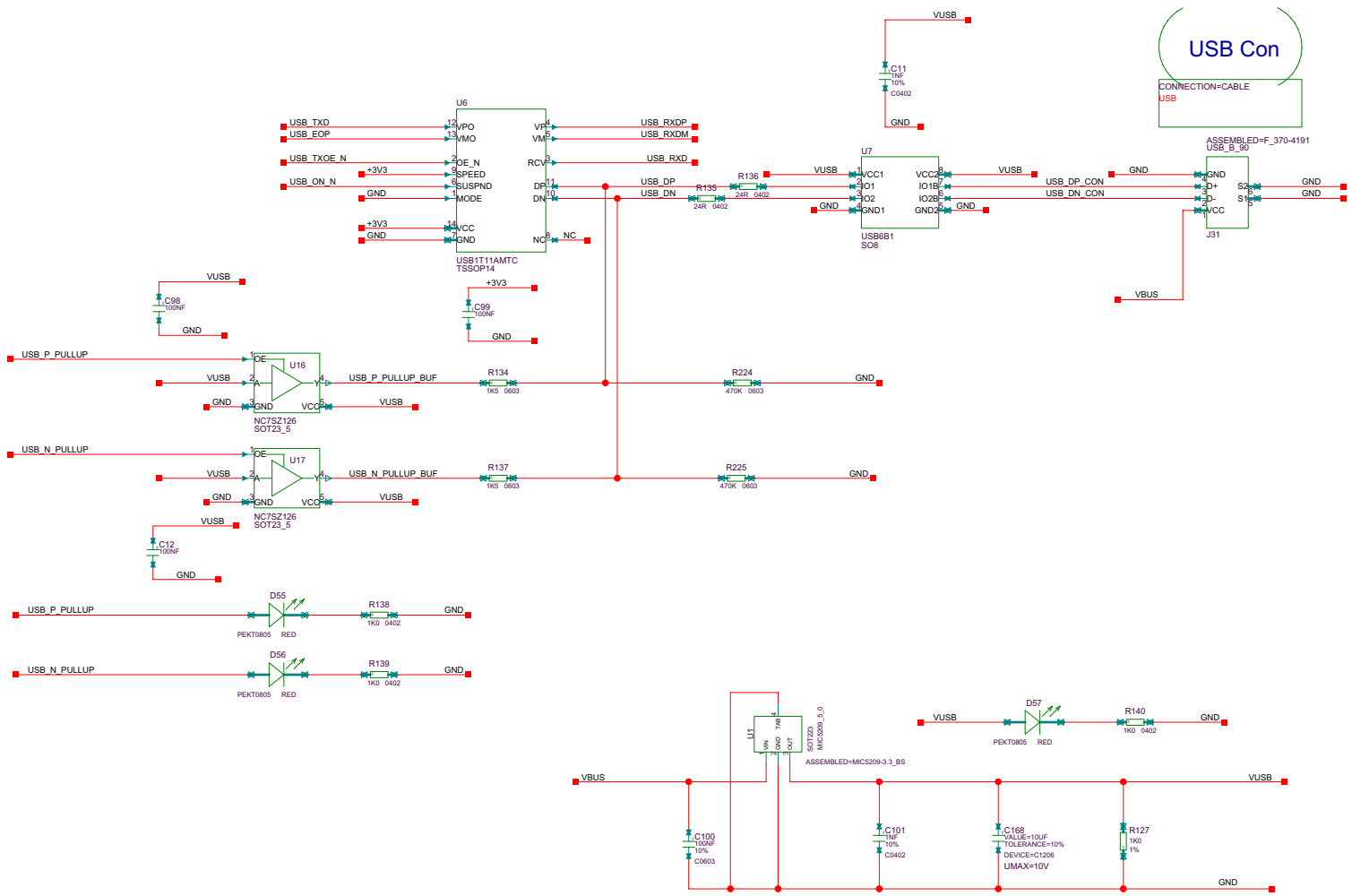

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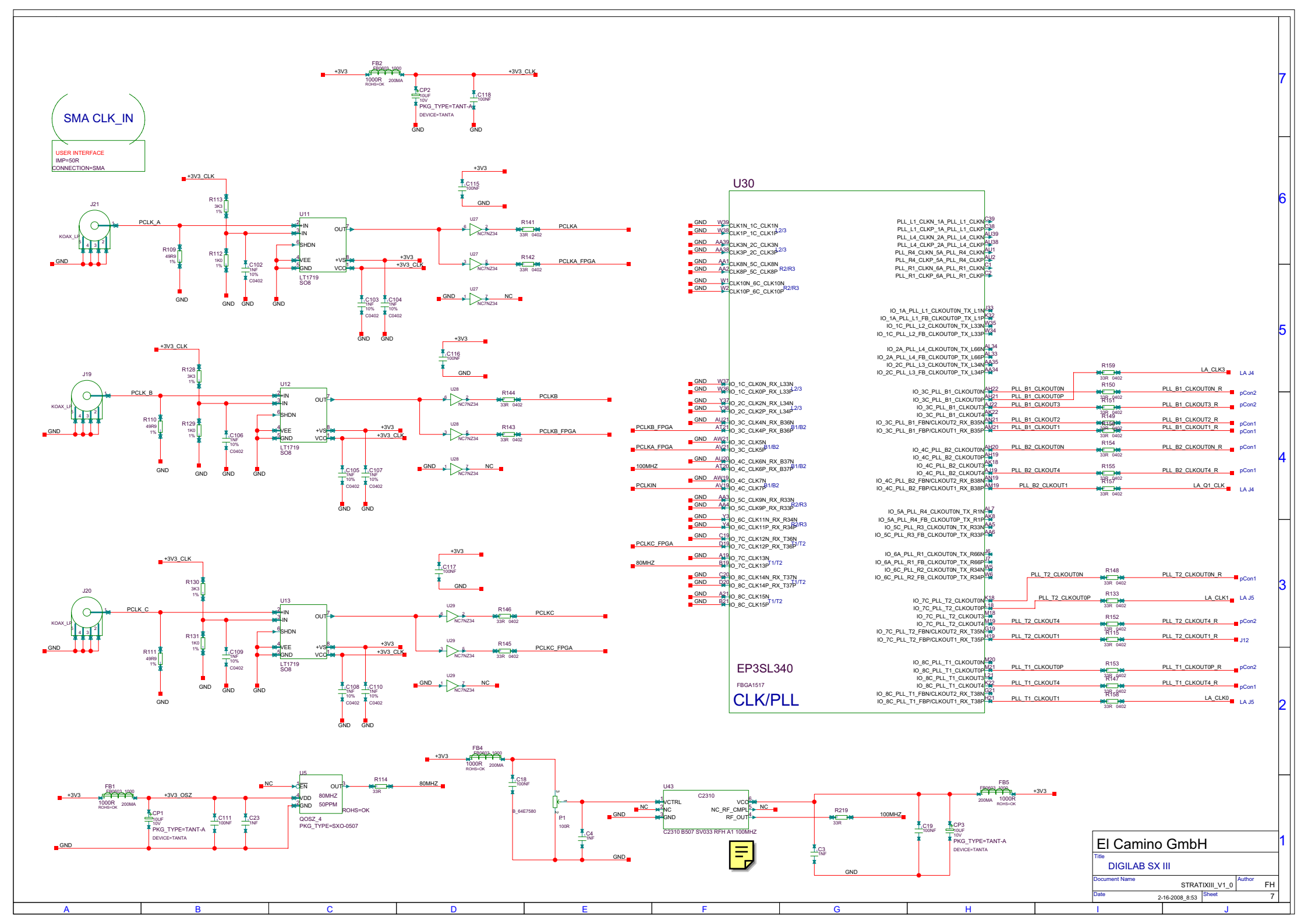
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CONNECTION=SMA
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FBGA1517
CLK/PLL
LT1719
SO8
NC7NZ34
C2310 B507 SV033 RFH A1 100MHZ
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PKG_TYPE=SXO-0507
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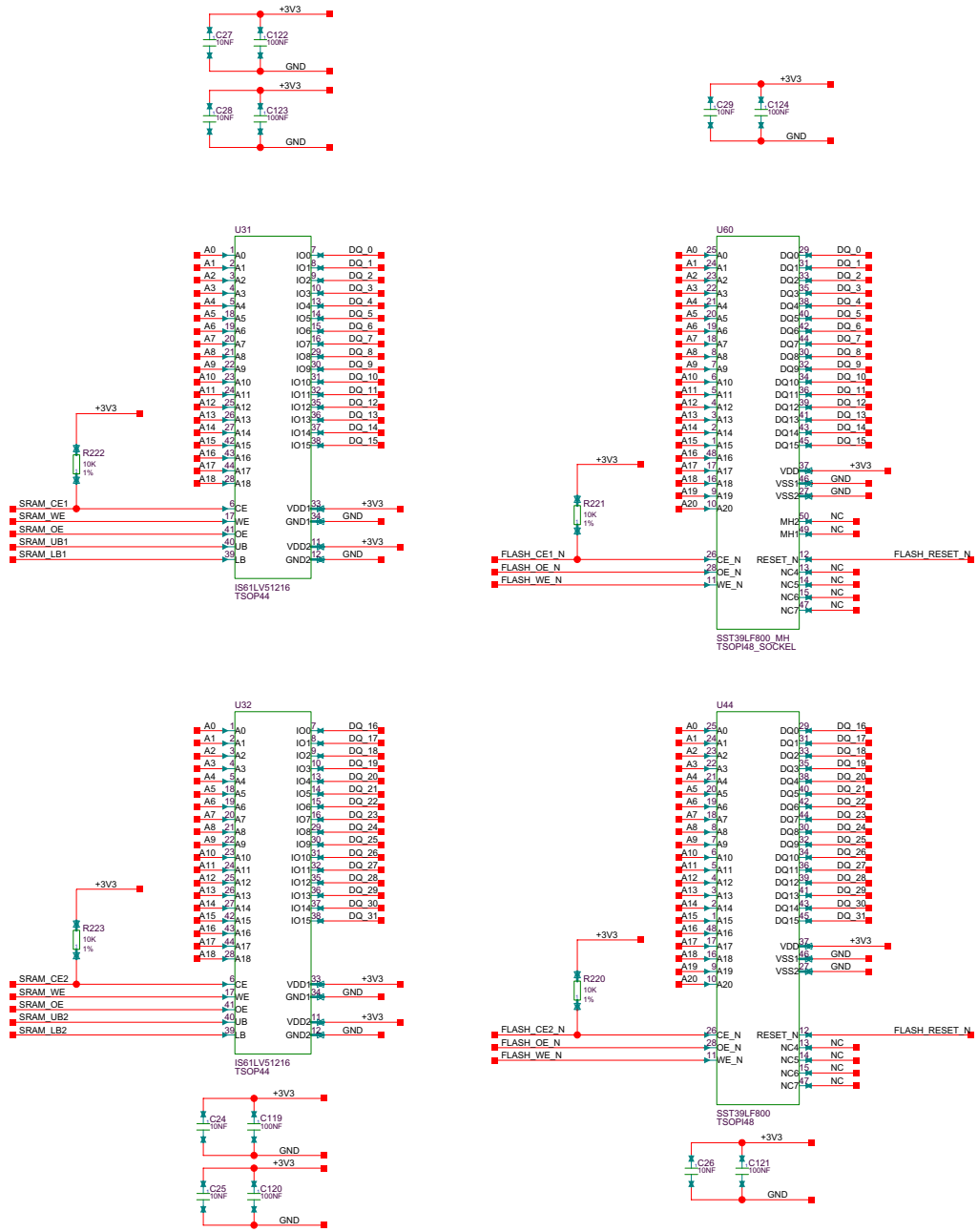

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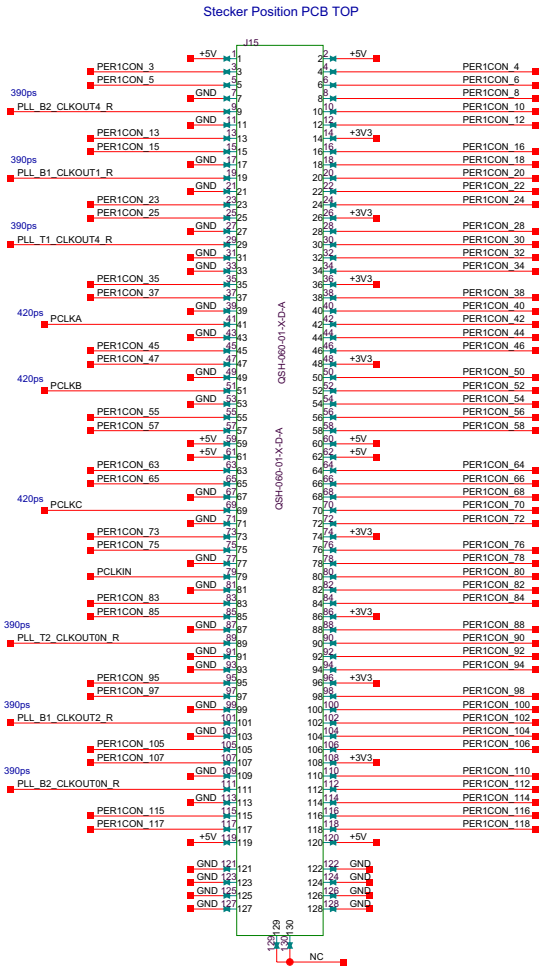

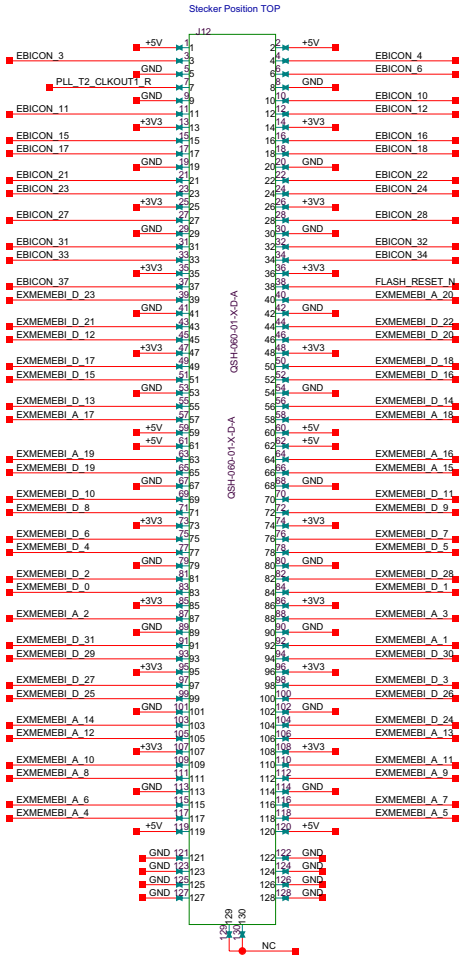

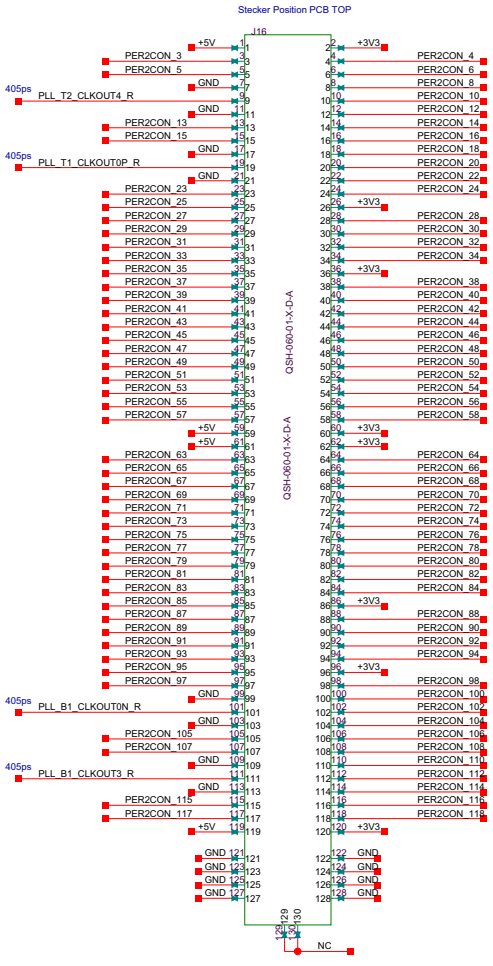

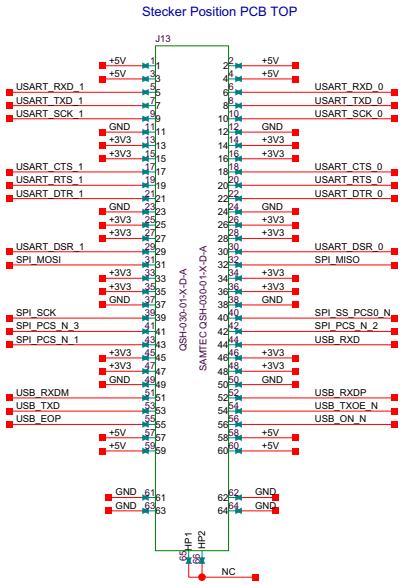

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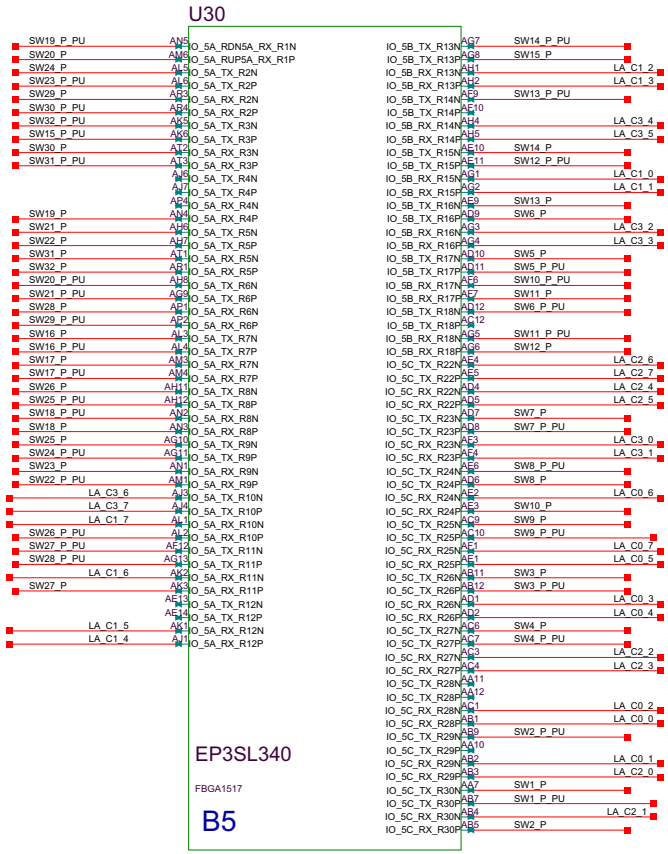

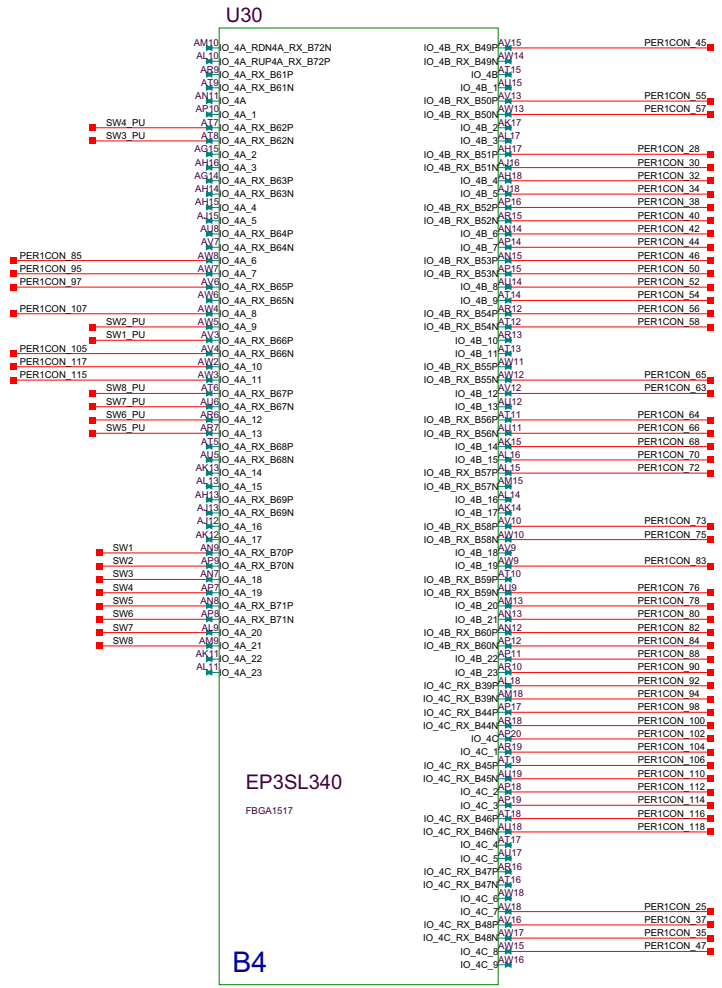

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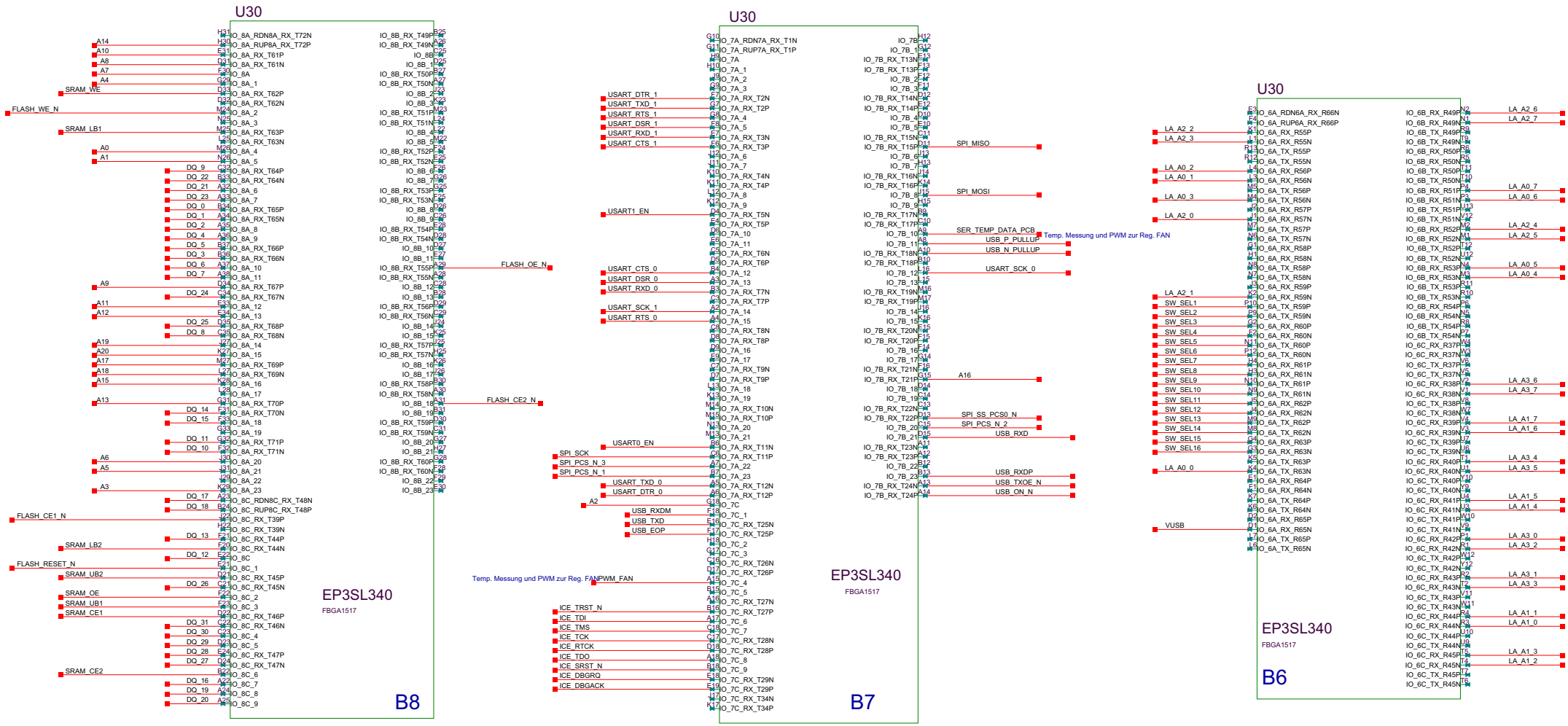

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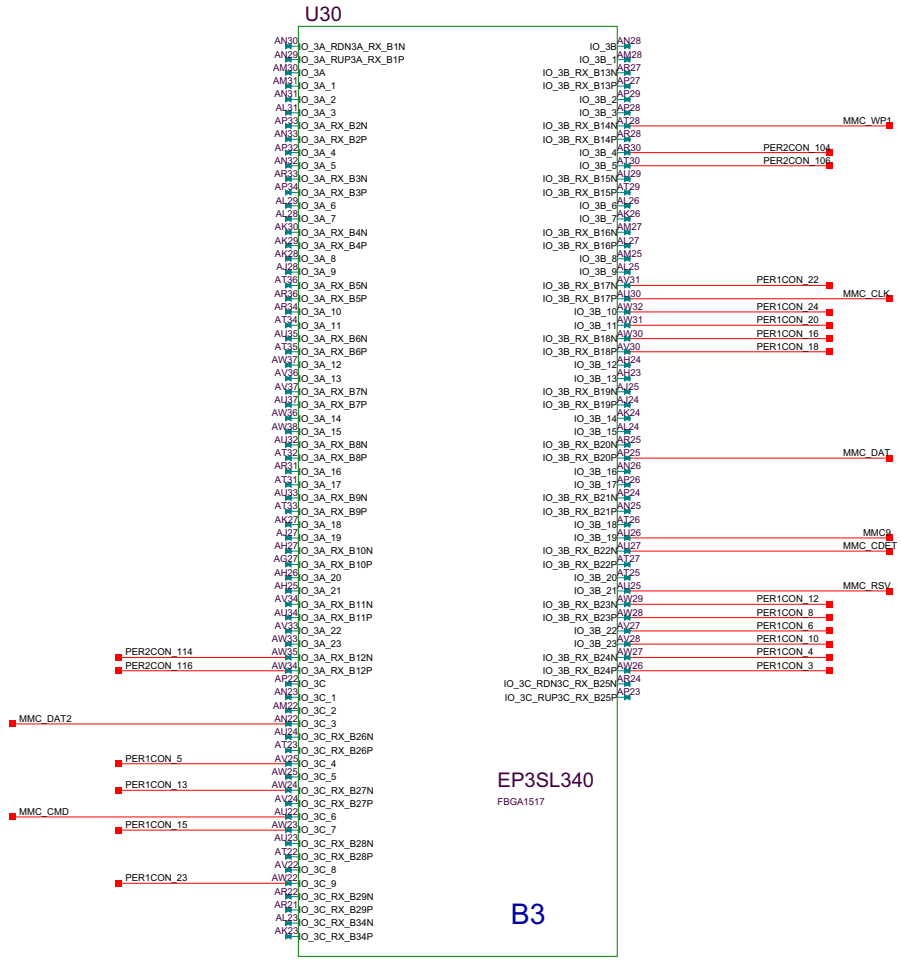

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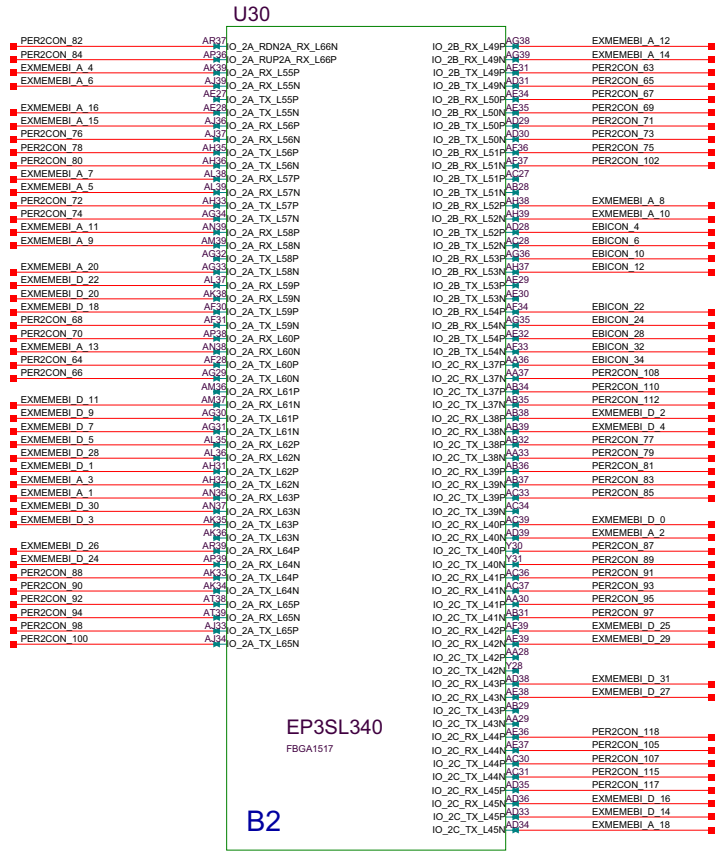

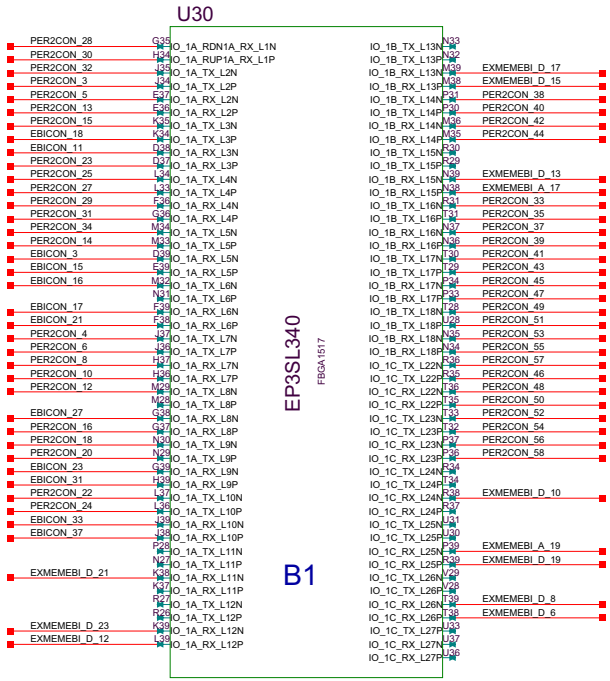

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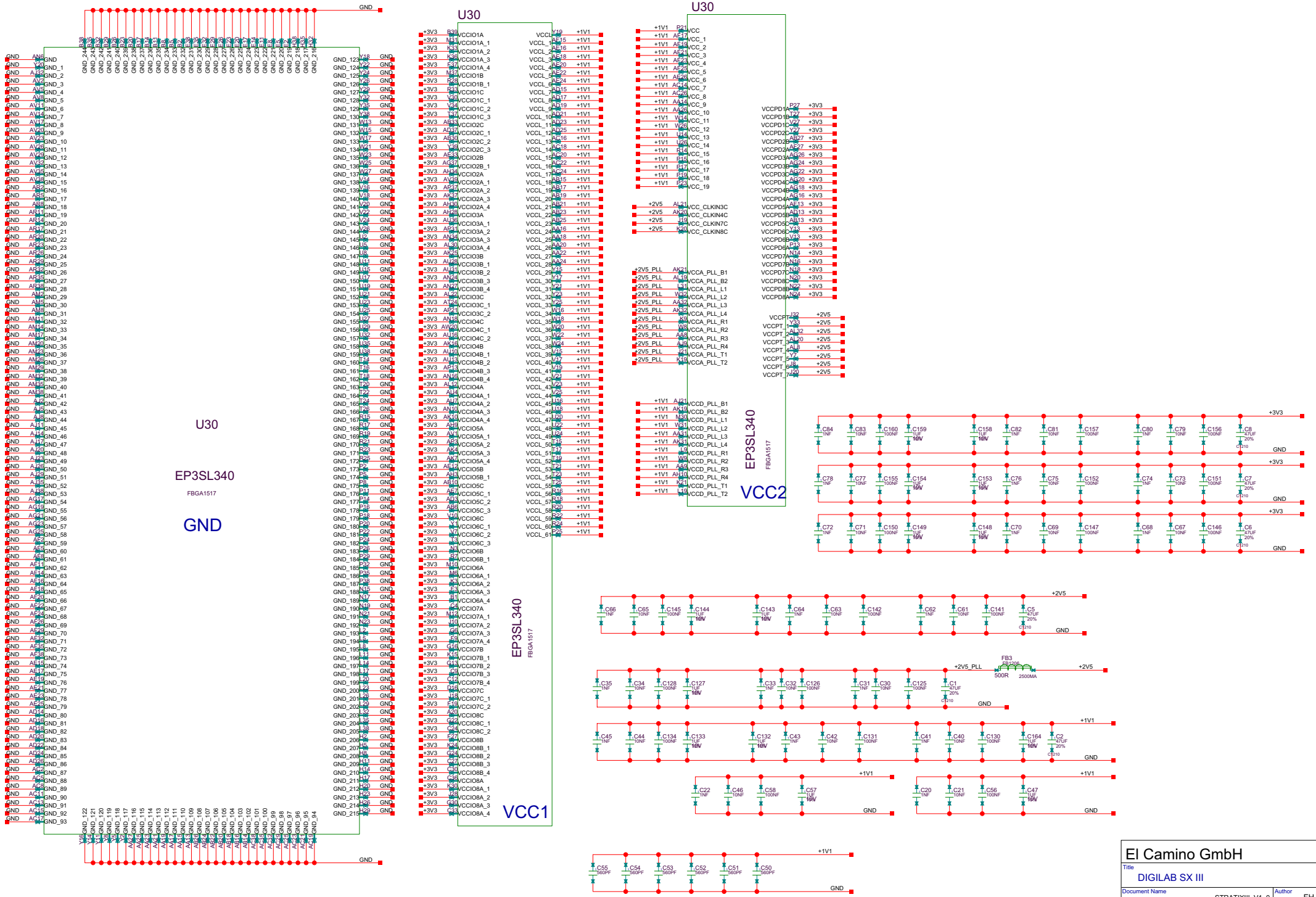
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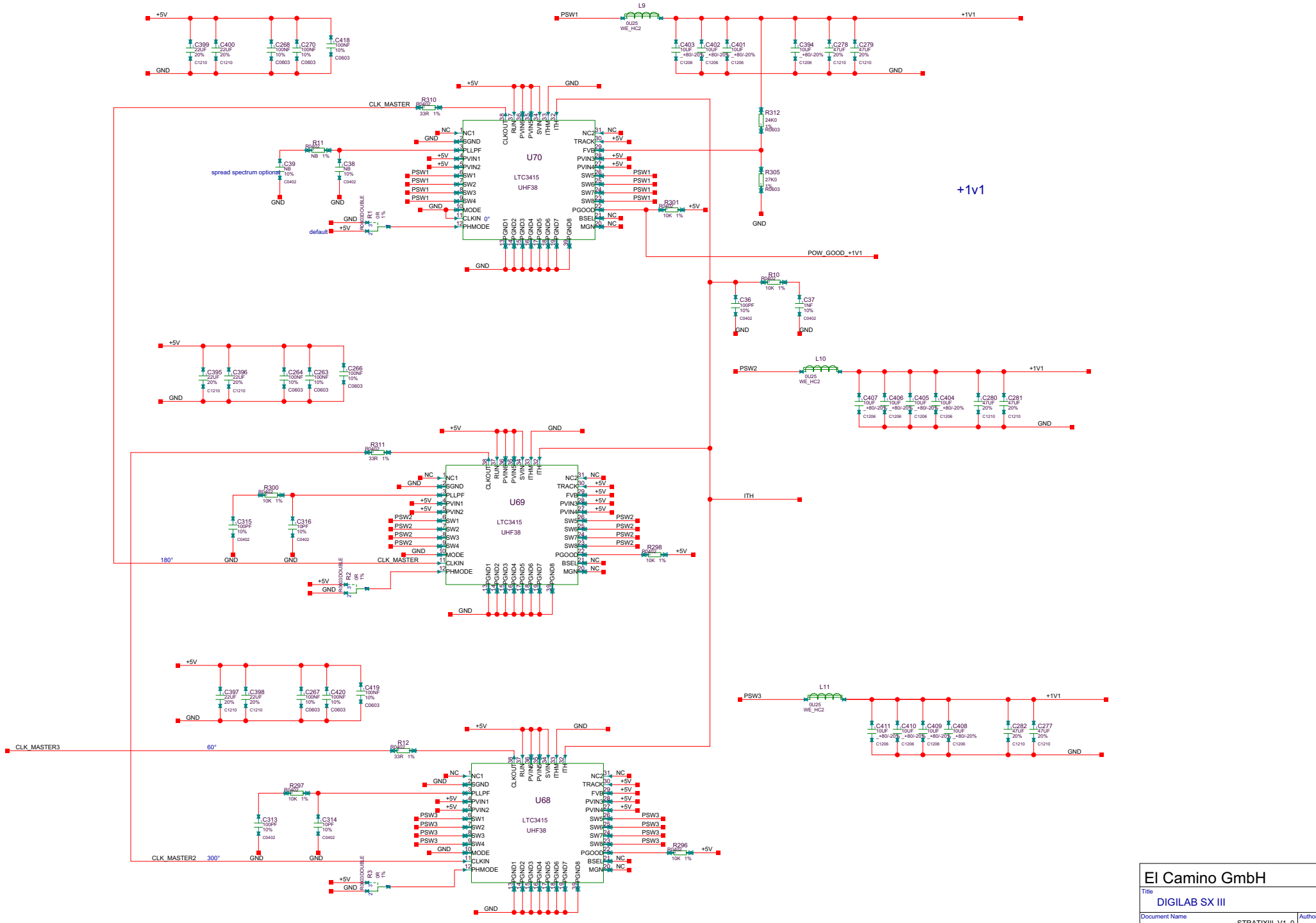
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U69
U68
LTC3415
UHF38
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default
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CLK_MASTER2
CLK_MASTER3
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60°
300°
ITH
POW_GOOD_+1V1
PSW1
PSW2
PSW3
L9
L10
L11
0U25
WE_HC2
+5V
GND
R310
R311
R312
R305
R301
R300
R298
R297
R296
R11
R10
R12
R1
R2
R3
C39
C38
C36
C37
C315
C316
C313
C314
C399
C400
C268
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C278
C279
C407
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C405
C404
C280
C281
C411
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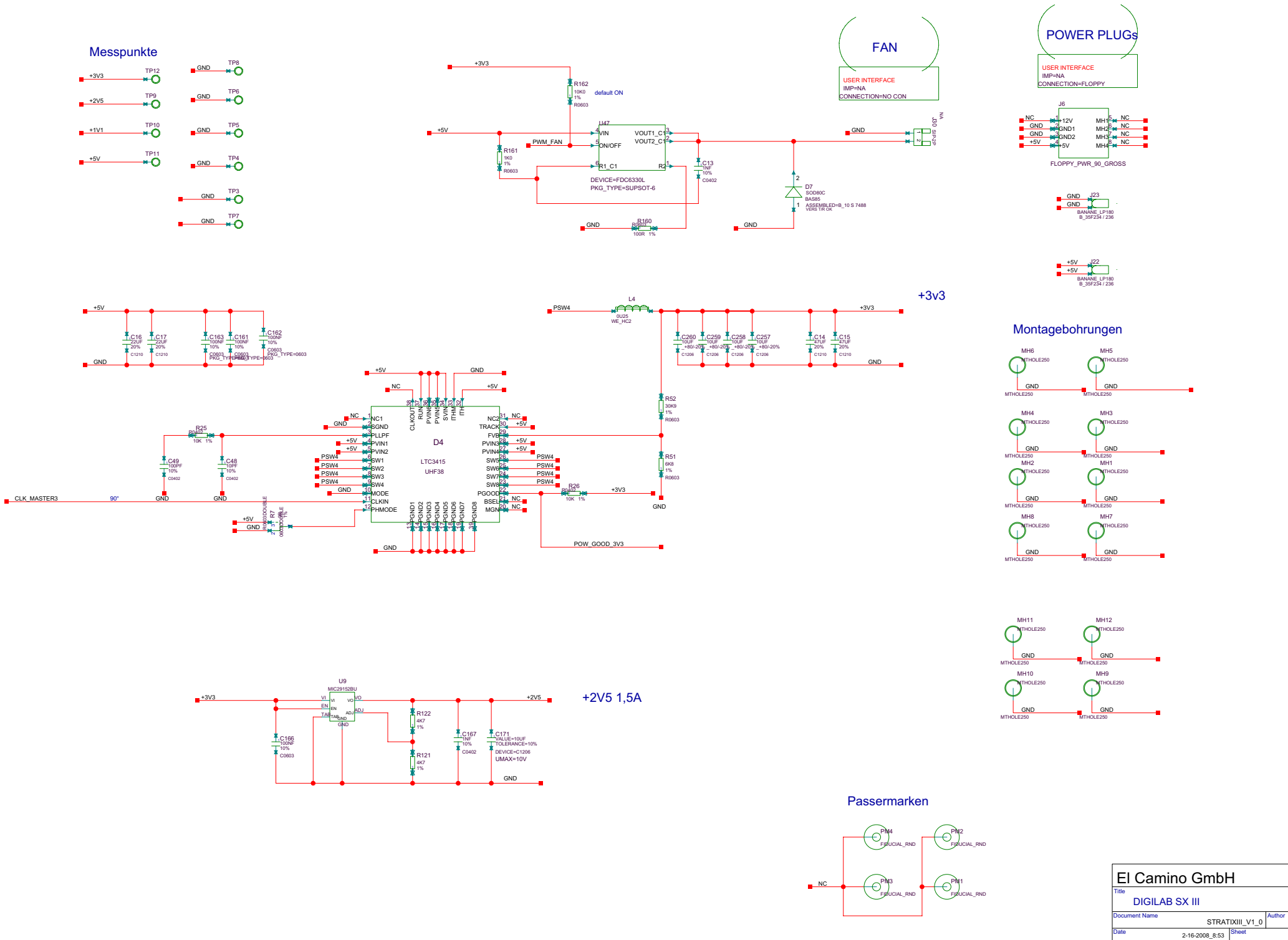
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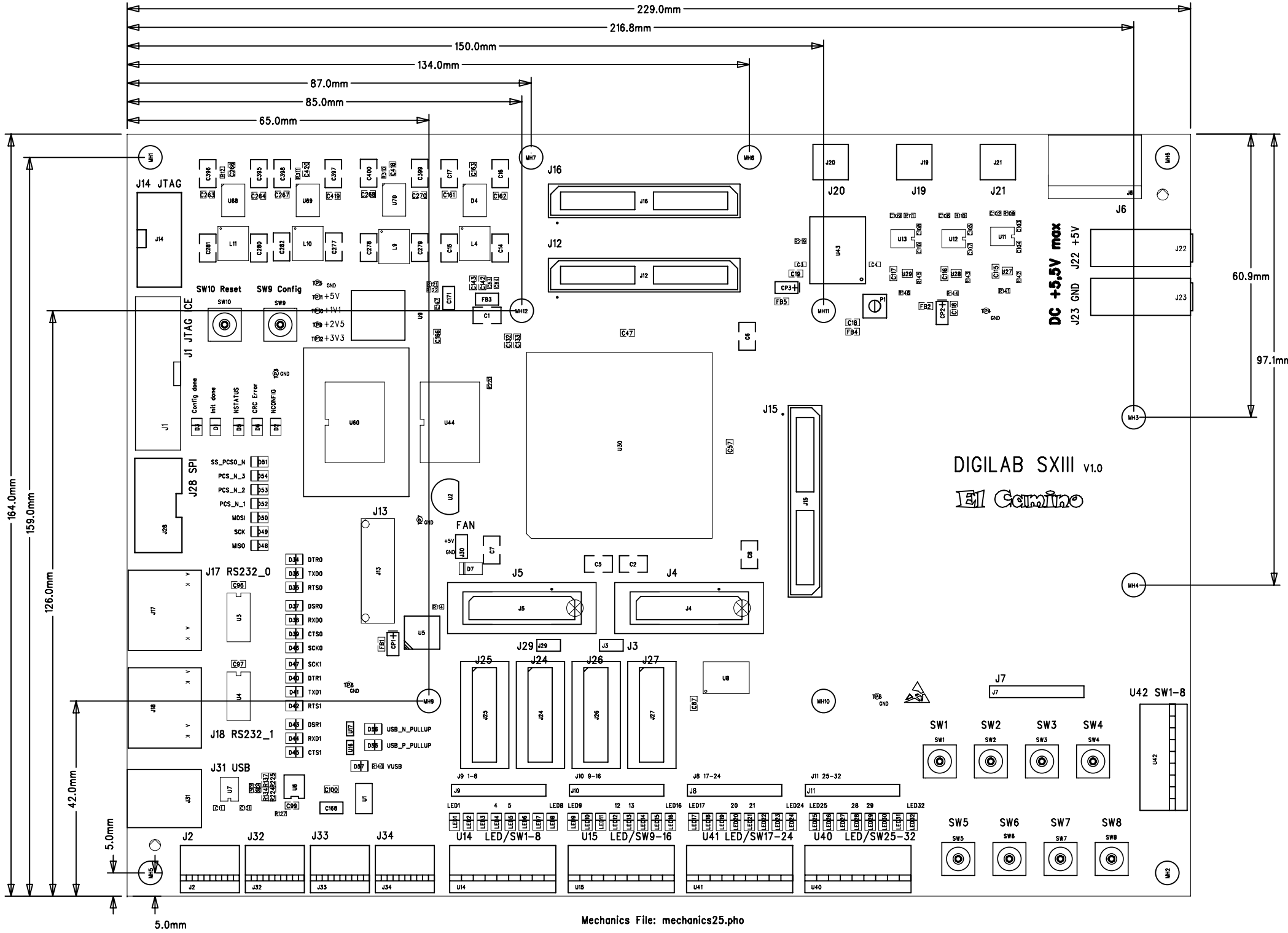

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