El Camino
Training - Engineering - Consultancy

DIGILAB SX V

Stratix V Prototyping Board

General Description

The DIGILAB SX V is a universal FPGA prototyping platform based on Altera's Stratix V device family. It can be used for ASIC prototyping, hardware evaluation or as a verification acceleration vehicle

Features

- Available with Altera Stratix V device in 1517 Pin FineLine BGA Package
  - 5SEEBH40C2 (standard)
  - 5SEE9 (on request)
- 338 user I/Os through
  - One Altera HSMC connector
  - Two Samtec QSH-060 (120 contact) connectors
  - Two 38 pin Mictor connectors
  - Nine DIL/SIL headers
- 2 MByte (512k x 32-bit) FLASH memory
- 2 MByte (512k x 32-bit) SRAM
- Configuration
  - EPCQ512 non-volatile configuration memory (AS x1 mode)
  - Push-buttons for reset and configuration
  - Various LEDs for configuration status
- User Interface
  - 32 three-state DIP switches with programmable pull-up/pull-down and 32 user LEDs
  - 16 two-state DIP switches
  - 8 push buttons, selectable low- or high active with programmable pull-up/pull-down
- Connector for SD/MMC cards
- JTAG connector for Altera download cable
- JTAG Multi-ICE connector
- Interfaces with monitoring LEDs
  - Two RS232 transceivers with 3-driver/3-receiver each
  - SPI interface connector
  - USB 1.1 transceiver (USB 2.0 support on request)
- Clocking
  - 80 MHz Crystal oscillator
  - 25 MHz Crystal oscillator
  - 3 SMA clock inputs
- Power supply circuitry
- FPGA controlled active heat sink and temperature sensor

Preface

Environmental Requirements

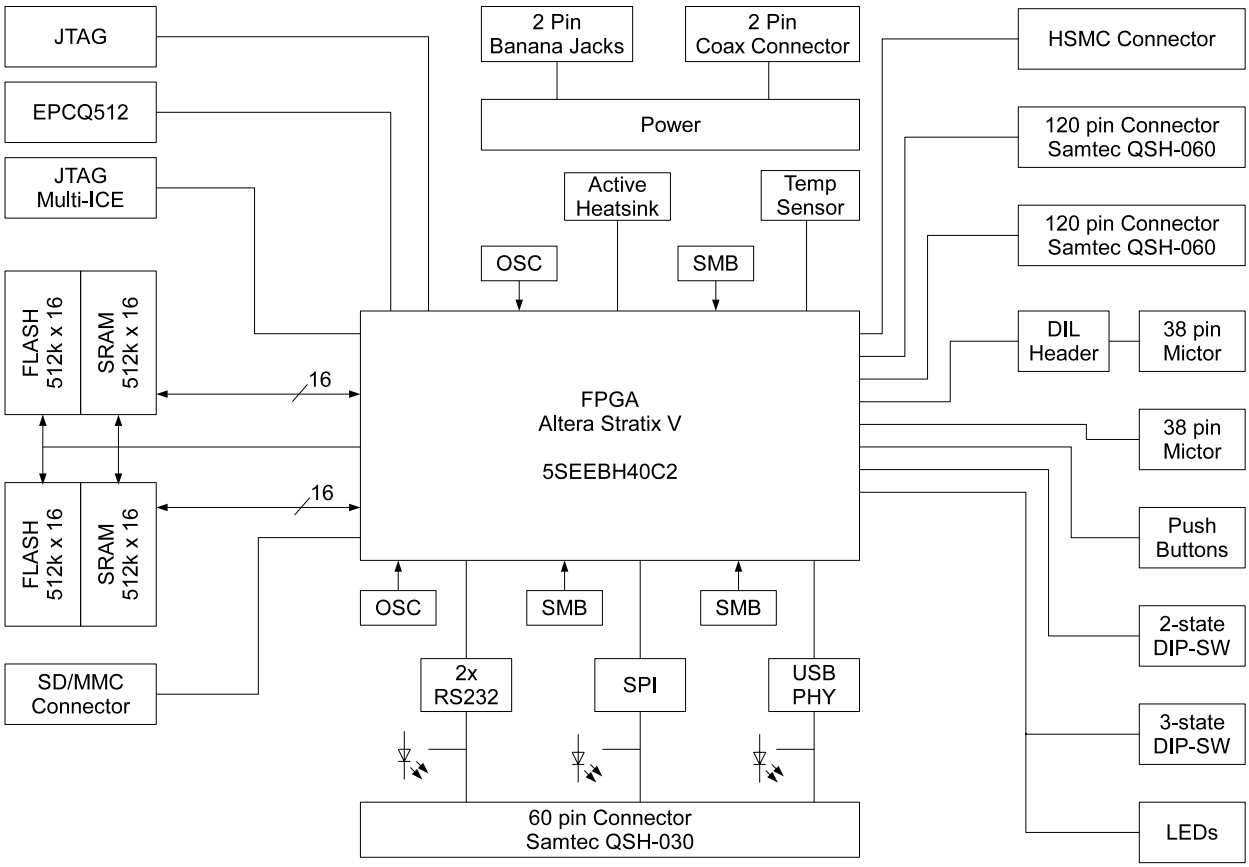
The development board must be stored between -40°C and 85°C. The recommended operating temperature is between 0°C and 70°C. Please contact El Camino for availability information on DIGILAB SX V boards that support the industrial temperature range of -40°C to 85°C.

The board can be damaged without proper anti-static handling.
Anti-static precautions should be taken before handling the board.

Functional Description

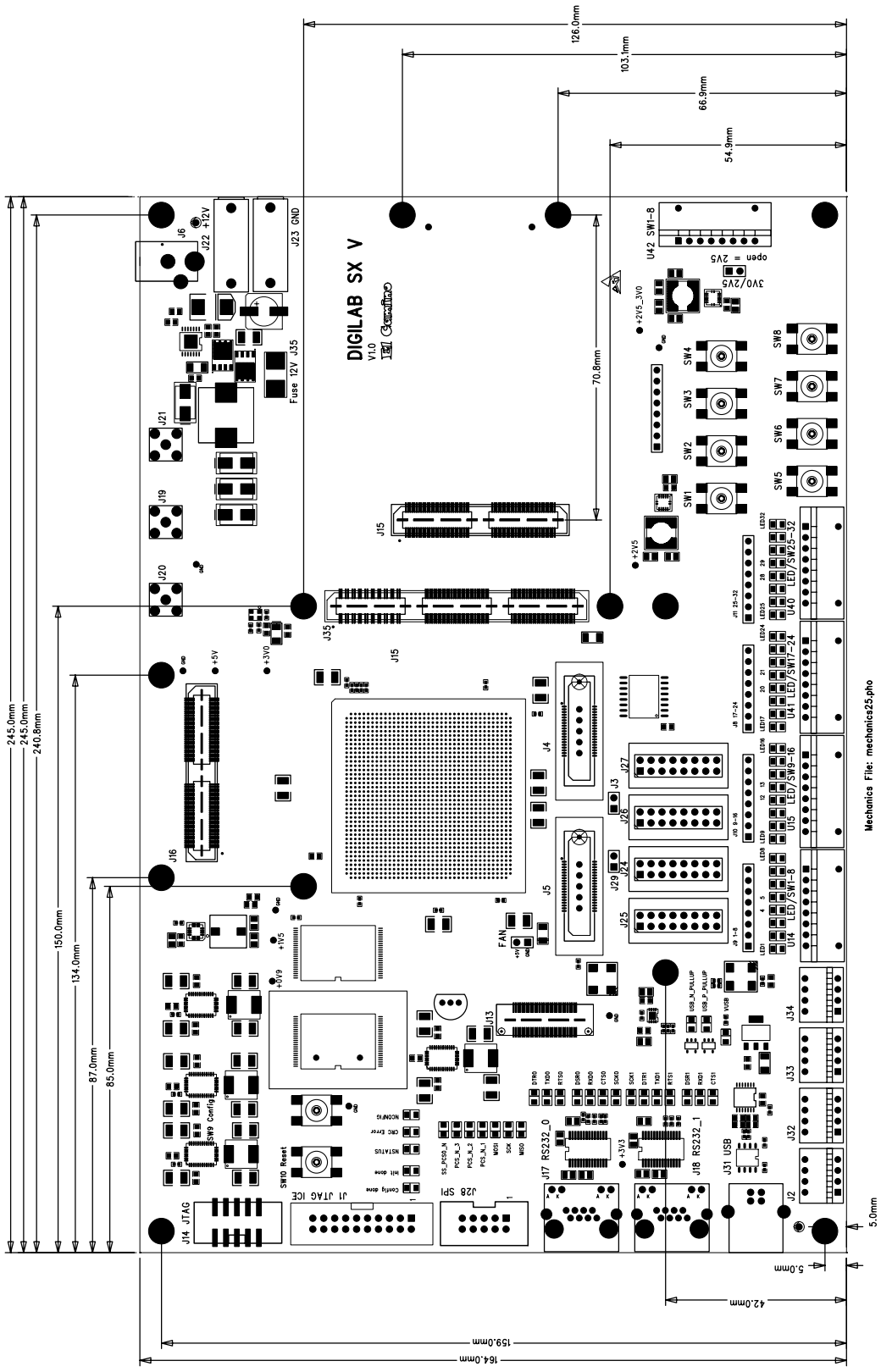
This section describes the elements of the DIGILAB SX V prototyping board. Figure 1 shows a block diagram of the board.

Figure 1: DIGILAB SX V Block Diagram



The DIGILAB SX V is a general purpose prototyping platform. Figure 2 shows the basic mechanical setup of the DIGILAB SX V. The measurements can be used to develop and manufacture custom adapter boards. Contact El Camino if you require further details on the mechanical dimensions of the board.

Figure 2: DIGILAB SX V Mechanical Setup - Top View



All measurements are in mm.

Stratix V Device

The DIGILAB SX V board can be equipped with any Stratix V device in a H40-H1517 FineLine BGA package with 696 IOs. Devices currently supported in this package are the 5SEE) and the 5SEEB. Furthermore it is possible to select any speed grade. Pricing and availability of the board will depend on the Stratix V device chosen. The standard device is the 5SEEBH40C2

Disable Unused Resources

When implementing custom user designs it is important to disable unused resources on the DIGILAB SX V, so that there are no bus contentions e.g. on the data bus connected to SRAM and FLASH.

In order to avoid contentions on the various switch and push button inputs it is recommended to either use the design template that is provided with the board or reserve all unused pins „As input tri-stated with weak pull-up resistor“. The board may be damaged if this guideline is not followed.

The SRAM and FLASH devices have pull-up resistors on their active low select lines.

Table 1: Disable Unused Resources

Function	Signal	Stratix V Pin	Value
SRAM	SRAM_CE1	AN11	’1’ or ’Z’
	SRAM_CE2	AH15	’1’ or ’Z’
FLASH	FLASH_CE1_N	AH10	’1’ or ’Z’
	FLASH_CE2_N	AV19	’1’ or ’Z’

Power Supply

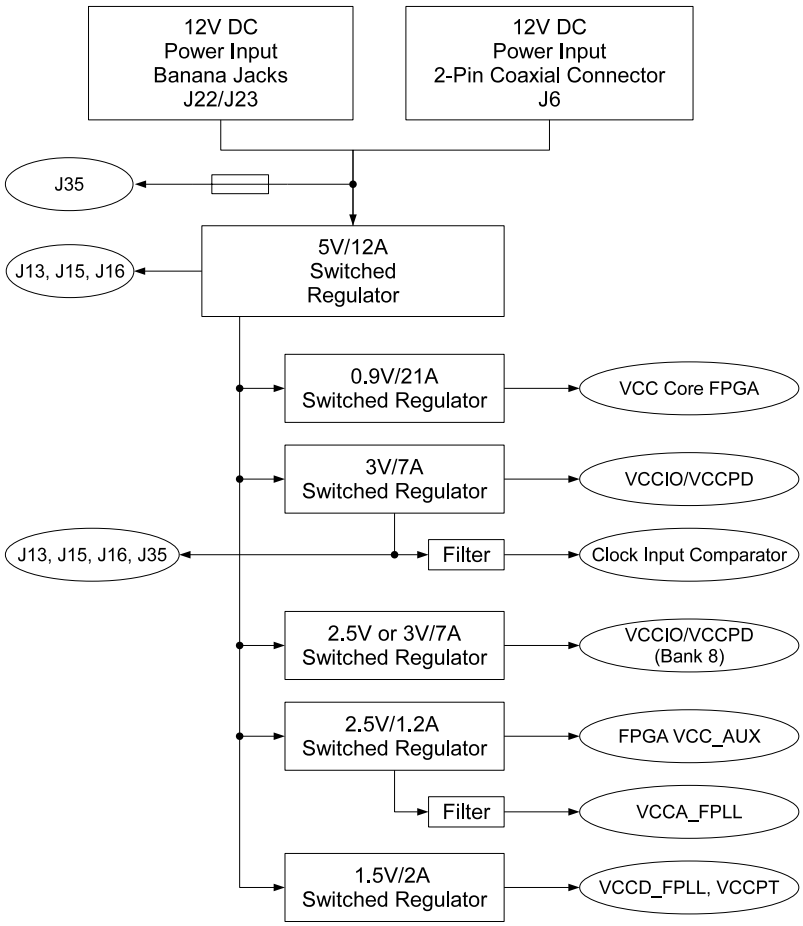
The DIGILAB SX V is meant to be used in a lab environment. It requires a 12V DC input and offers two optional power connectors. Power can be supplied through two banana jacks or a coaxial two pin power connector.

Table 2: Power Supply Options

Option	Voltage	Connector	Description
Banana Jacks	12V DC	J22 (red) +12V J23 (black) GND	For use with a Lab power supply
2-Pin Coaxial Connector	12V DC	J6	For use with a standard power adapter (positive tip polarity)

The DC input current when unconfigured and during configuration is a approximately *450* mA at 12V DC. The input current while the maintenance design is running and during self-test is approximately *550* mA.

Figure 3: DIGILAB SX V Power Supply



Thermal considerations

The total power consumption can vary significantly, depending on the implemented design and the clock frequencies. Refer to information from Altera for details on Stratix V power consumption. We strongly recommend to do a power analysis and/or monitor the Stratix V case temperature during operation.

Depending on the design implemented and the total power consump-

tion, active cooling may be necessary. A 5V DC cooling fan is connected to J30. The fan can be controlled from within the FPGA by driving the PWM_FAN signal. Furthermore, the board is equipped with an active temperature sensor that is mounted with a thermal adhesive to the board in close proximity to the FPGA. The board comes with an encrypted IP function, that reads the temperature once per second and controls the cooling fan. The IP function has the following IO ports and parameters and can be instantiated in a user design. Alternatively the fan control signal PWM_FAN can be left floating or driven high to permanently turn on the fan. During configuration the fan will be on, which gives some feedback on the functionality of the fan at each power or configuration cycle.

Figure 4: Fan Control

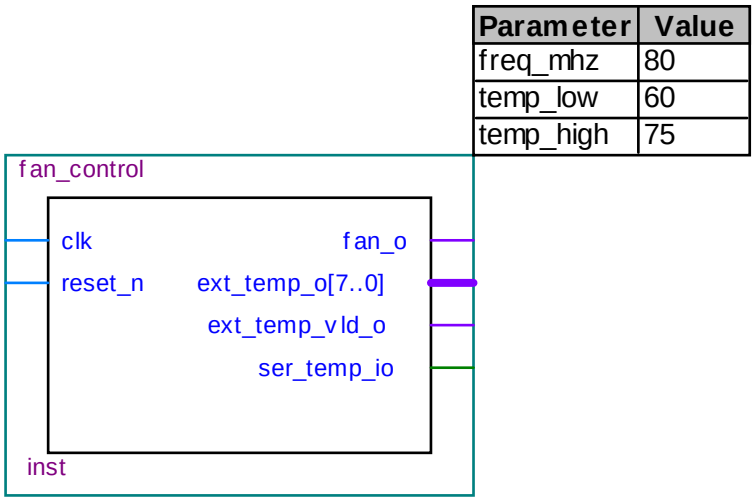


Table 3: Fan Control Ports and Parameters

	Name	Direction	Function
Parameter	freq_mhz	in	Specifies the clock frequency in MHz. Used to calculate timing for accessing the temperature sensor
	temp_low	in	Temperature in degree Celsius at which the fan will start to receive PWM pulses
	temp_high	in	Temperature in degree Celsius at which the fan will be fully turned on
Ports	clk	in	Clock input
	reset_n	in	Low active reset input, de-assertion should be synchronized to clk externally
	fan_o	out	Control signal for the fan; should be connected to PWM_FAN on the board
	ext_temp_o[7..0]	out	Actual temperature in degree Celsius (signed), valid while ext_temp_vld_o is high
	ext_temp_vld_o	out	High while ext_temp_o is valid
	ser_temp_io	inout	Interface to the temperature sensor, connect to SER_TEMP_DATA_PCB through a bi-directional pin

SRAM

U31 and U32 are two 1 MByte (512k x 16) asynchronous SRAM devices. They are connected to the Stratix V device so that they can be used by any custom logic in the FPGA or by a Nios II processor as general-purpose memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The SRAM shares a common bus with the on-board FLASH devices.

A data sheet for the SSRAM devices can be found at:
URL: http://www.alliancememory.com
Type: AS7C38098A

The pinout can be found in the following table or it can be extracted from the netlist, that comes with the board.

CFI Flash Memory

U60 and U44 are two 1 MByte (512k x 16) CFI FLASH memory devices that can be used as a general purpose, non-volatile storage. They are connected to the Stratix V device so that they can be used by any custom logic in the FPGA or by a Nios II processor as general-purpose, non-volatile memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The FLASH devices share a common bus with the on-board SRAM devices.

A data sheet for the Flash memory devices can be found at:
URL: http://www.sst.com
Type: SST39VF800A

The pinout can be found in the following table or it can be extracted from the netlist, that comes with the board.

Table 4: Memory Signals - SRAM U31/U32 and FLASH U60/U44

Signal	Stratix V U30	SRAM	FLASH	Signal	Stratix III U30	SRAM	FLASH
DQ_0	AM14	U31	U60	A0	AJ6	both	both
DQ_1	AN14	U31	U60	A1	AV8	both	both
DQ_2	AH12	U31	U60	A2	AN10	both	both
DQ_3	AN12	U31	U60	A3	AG10	both	both
DQ_4	AJ12	U31	U60	A4	AW8	both	both
DQ_5	AG12	U31	U60	A5	AV10	both	both
DQ_6	AL12	U31	U60	A6	AW10	both	both
DQ_7	AK12	U31	U60	A7	AV11	both	both
DQ_8	AK11	U31	U60	A8	AN8	both	both
DQ_9	AH13	U31	U60	A9	AL11	both	both
DQ_10	AM13	U31	U60	A10	AR6	both	both
DQ_11	AL13	U31	U60	A11	AR9	both	both
DQ_12	AM10	U31	U60	A12	AU7	both	both
DQ_13	AJ10	U31	U60	A13	AU8	both	both
DQ_14	AP12	U31	U60	A14	AT9	both	both
DQ_15	AN15	U31	U60	A15	AT17	both	both
DQ_16	AP10	U32	U44	A16	AU17	both	both
DQ_17	AG9	U32	U44	A17	AT18	both	both
DQ_18	AH9	U32	U44	A18	AU9	both	both
DQ_19	AN9	U32	U44	A19	AR11		both
DQ_20	AP9	U32	U44	A20	AJ7		both
DQ_21	AR15	U32	U44	SRAM_WE	AP6	both	
DQ_22	AR14	U32	U44	SRAM_OE	AU16	both	
DQ_23	AP15	U32	U44	SRAM_CE1	AN11	U31	
DQ_24	AU10	U32	U44	SRAM_LB1	AM8	U31	
DQ_25	AT11	U32	U44	SRAM_UB1	AM11	U31	
DQ_26	AU11	U32	U44	SRAM_CE2	AH15	U32	
DQ_27	AT12	U32	U44	SRAM_LB2	AT15	U32	
DQ_28	AU12	U32	U44	SRAM_UB2	AU15	U32	
DQ_29	AR12	U32	U44	FLASH_OE_N	AP18		both
DQ_30	AT14	U32	U44	FLASH_WE_N	AV13		both
DQ_31	AU14	U32	U44	FLASH_CE1_N	AH10		U60
				FLASH_CE2_N	AV19		U44

RS-232 Serial Interfaces

The DIGILAB SX V provides two independent bidirectional RS-232 serial I/O interfaces. The board contains the transceiver (U3, U4), however the logic controller (UART) must be implemented in the Stratix V device.

J17 and J18 are standard RJ45 connectors. These connectors can be used for communication with a host computer using an adapter cable to connected for example to a COM port. In addition, all RS-232 signals are available through J13, a Samtec QSH-30 connector, which allows to connect custom add-on or interface boards.

J17 and J18 can transmit all RS-232 signals. The Stratix V design may use only signals it needs, such as RXD and TXD. LEDs are connected to all RS232 signals, giving a visual indication, whether data is being transmitted or received. The following table shows the pin mapping between the Stratix V device and the RS232 signals.

A data sheet for the RS-232 transceiver can be found at:
URL: http://www.maxim-ic.com
Type: MAX3238

Table 5: RS-232 Interfaces

Interface	Function	Stratix V - U30		RJ45 Connector	Samtec Connectors J13
		Signal	Pin		
J17 RS232_0	DTR	USART_DTR_0	AM17	J17 - 1, 2	22
	TXD	USART_TXD_0	AG16	J17 - 5	8
	RTS	USART_RTS_0	AU18	J17 - 7	20
	DSR	USART_DSR_0	AP19	J17 - 3	30
	RXD	USART_RXD_0	AR19	J17 - 6	6
	CTS	USART_CTS_0	AR18	J17 - 8	18
	Enable	USART0_EN	AW19	n/a	n/a
	n/a	USART_SCK_0	AV17	n/a	10
J18 RS232_1	DTR	USART_DTR_1	AE19	J18 - 1, 2	21
	TXD	USART_TXD_1	AD18	J18 - 5	7
	RTS	USART_RTS_1	AD17	J18 - 7	19
	DSR	USART_DSR_1	AL18	J18 - 3	29
	RXD	USART_RXD_1	AM19	J18 - 6	5
	CTS	USART_CTS_1	AN19	J18 - 8	17
	Enable	USART1_EN	AN18	n/a	n/a
	n/a	USART_SCK_1	AA15	n/a	9

SPI Interface

The DIGILAB SX V provides an SPI interface through general purpose Stratix V I/O pins. Besides an ESD protection, there are no special buffers or level shifters implemented. In order to use the SPI interface, a logic controller for SPI must be implemented in the Stratix V device.

The SPI interface is available through J28, a standard dual row 2x5 header. In addition, all SPI signals are available through J13, a Samtec QSH-30 connector, which allows to connect custom add-on or interface boards.

LEDs are connected to all SPI signals, giving a visual indication, whenever data is being transmitted or received. The following table shows the pin mapping between the Stratix V device and the SPI signals.

Table 6: SPI Interface

Function	Stratix V - U30		J28 2x5 Header	Samtec Connectors J13
	Signal	Pin		
GND	n/a	n/a	1	n/a
GND	n/a	n/a	2	n/a
3.3V	n/a	n/a	3	n/a
SCK	SPI_SCK	AL16	4	39
MISO	SPI_MISO	AD16	5	32
MOSI	SPI_MOSI	AA14	6	31
PCS_2	SPI_PCS_N_2	AW13	7	42
PCS_3	SPI_PCS_N_3	AM16	8	41
PCS_0	SPI_SS_PCS0_N	AW17	9	40
PCS_1	SPI_PCS_N_1	AF16	10	43

USB Interface

On the board, there is a USB transceiver that complies with USB 1.1, as well as a USB connector and a line protection device. USB 2.0 can be supported with a different, pin-compatible transceiver, that can be mounted on a request basis. The board provides the transceiver (U6), however the USB controller must be implemented in the Stratix V device.

J31 is a standard USB Type B connector. This connector can be used for communication with a host computer using a standard USB cable. In addition, the local signals of the USB transceiver are available through J13, a Samtec QSH-30 connector, which allows to connect custom add-on or interface boards.

LEDs are connected to the USB data signals, giving a visual indication whenever data is being transmitted. Furthermore, there is a LED (D57) that monitors the USB input voltage.

The USB interface has programmable pull-up resistors. They can be controlled through the signals USB_P_PULLUP (monitored through LED D55) and USB_N_PULLUP (monitored through LED D56) from within the FPGA.
Furthermore the presence of the USB 5V voltage can be monitored with LED D57 and the FPGA input VUSB.

A data sheet for the USB transceiver can be found at:
URL: http://www.fairchildsemi.com
Type: USB1T11A (for USB 2.0: USB1T20)

The following table shows the pin mapping between the Stratix V device and the USB signals.

Table 7: USB Interface

Function	Stratix V - U30		Samtec Connectors J13
	Signal	Pin	
VPO	USB_TXD	AP16	53
VMO	USB_EOP	AR17	55
OE_N	USB_TXOE_N	AL10	54
SUSPND	USB_ON_N	AF10	56
VP	USB_RXDP	AW14	52
VM	USB_RXDM	AN16	51
RCV	USB_RXD	AV14	44
D+ Pull-Up	USB_P_PULLUP	AV16	n/a
D- Pull-Up	USB_N_PULLUP	AW16	n/a
VBUS Monitor	VUSB	AP13	n/a

Multi-ICE JTAG Interface

The Multi-ICE JTAG connector allows the connection of a Multi-ICE interface unit to the board. The connection enables debugging of ARM processors implemented inside the Stratix V FPGA. All signals feature ESD protection and are directly connected to standard Stratix V I/O pins. The signal mapping can be found in the following table:

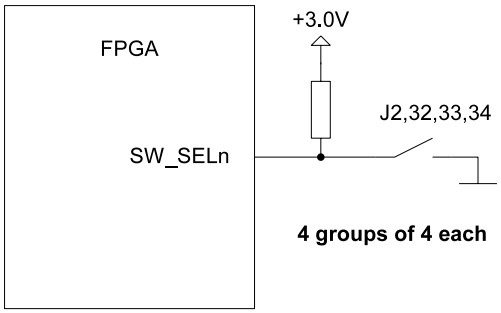
Table 8: Multi-ICE JTAG Connector

Signal	J1 Connector		Signal	Stratix V U30 Pin
	Pin	Pin		
3.0V	2	1	3.0V	n/a
GND	4	3	ICE_TRST_N	AG19
GND	6	5	ICE_TDI	AH19
GND	8	7	ICE_TMS	AJ19
GND	10	9	ICE_TCK	AK18
GND	12	11	ICE_RTCK	AH18
GND	14	13	ICE_TDO	AJ18
GND	16	15	ICE_SRST_N	AF19
GND	18	17	ICE_DBGRQ	AG18
GND	20	19	ICE_DBGACK	AE18

DIP Switches (two-state)

The DIGILAB SX V has 16 two-state DIP switches. They switch between GND (when on) and a 10k Ohm pull-up resistor (when off). The following diagram shows the functionality of the two-state switches.

Figure 5: Two-state DIP switches



The signal mapping for the 2-state DIP switches can be found in the following table:

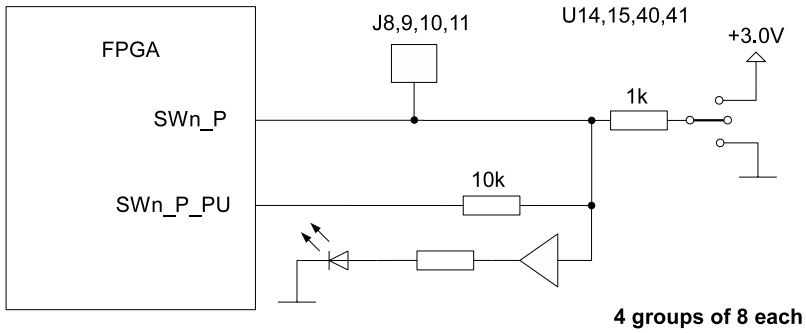
Table 9: DIP Switches (two-state)

DIP Switch		Signal	Stratix V - U30 Pin
J2	1	SW_SEL1	AL29
	2	SW_SEL2	AM29
	3	SW_SEL3	AK29
	4	SW_SEL4	AJ29
J32	1	SW_SEL5	AP28
	2	SW_SEL6	AR28
	3	SW_SEL7	AL27
	4	SW_SEL8	AL28
J33	1	SW_SEL9	AM28
	2	SW_SEL10	AN28
	3	SW_SEL11	AA26
	4	SW_SEL12	AA27
J34	1	SW_SEL13	AA28
	2	SW_SEL14	AA29
	3	SW_SEL15	AB27
	4	SW_SEL16	AC27

DIP Switches (three-state) and User LEDs

The DIGILAB SX III has a total of 32 three-state DIP switches in four groups of eight.

Figure 6: Three-state DIP switches



The signals driven by these switches are also connected to programmable pull-up/down resistors, as well as LEDs through drivers. The FPGA signal SWn_P can be used as an input, driven by the switch and pulled high or low through SWn_P_PU. Alternatively, when the switch is not used, the signal SWn_P can be used as output driven by the FPGA and controlling the LED. The LEDs will show the current status of the line.

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Table 10: Three-state DIP switches and LEDs

Switch		LED	Signal		Pull-Up/Down Resisotr	
			Name	Stratix V U30 - Pin	Name	Stratix V U30 - Pin
U14	1	LED1	SW1_P	AL21	SW1_P_PU	AL15
	2	LED2	SW2_P	AL14	SW2_P_PU	AJ15
	3	LED3	SW3_P	AP22	SW3_P_PU	AW22
	4	LED4	SW4_P	AU23	SW4_P_PU	AT23
	5	LED5	SW5_P	AG23	SW5_P_PU	AD22
	6	LED6	SW6_P	AF23	SW6_P_PU	AG22
	7	LED7	SW7_P	AR22	SW7_P_PU	AJ20
	8	LED8	SW8_P	AL20	SW8_P_PU	AJ21
U15	1	LED9	SW9_P	AW23	SW9_P_PU	AV22
	2	LED10	SW10_P	AV23	SW10_P_PU	AE22
	3	LED11	SW11_P	AF22	SW11_P_PU	AK21
	4	LED12	SW12_P	AL22	SW12_P_PU	AD23
	5	LED13	SW13_P	AE23	SW13_P_PU	AM23
	6	LED14	SW14_P	AN23	SW14_P_PU	AM22
	7	LED15	SW15_P	AN22	SW15_P_PU	AU27
	8	LED16	SW16_P	AU25	SW16_P_PU	AR24
U41	1	LED17	SW17_P	AT24	SW17_P_PU	AP25
	2	LED18	SW18_P	AN24	SW18_P_PU	AN25
	3	LED19	SW19_P	AT26	SW19_P_PU	AD27
	4	LED20	SW20_P	AE27	SW20_P_PU	AH25
	5	LED21	SW21_P	AU26	SW21_P_PU	AV25
	6	LED22	SW22_P	AP27	SW22_P_PU	AE25
	7	LED23	SW23_P	AC24	SW23_P_PU	AH27
	8	LED24	SW24_P	AG27	SW24_P_PU	AB24
U40	1	LED25	SW25_P	AP24	SW25_P_PU	AM25
	2	LED26	SW26_P	AR25	SW26_P_PU	AF25
	3	LED27	SW27_P	AH24	SW27_P_PU	AD24
	4	LED28	SW28_P	AW25	SW28_P_PU	AE24
	5	LED29	SW29_P	AJ27	SW29_P_PU	AU24
	6	LED30	SW30_P	AV26	SW30_P_PU	AK27
	7	LED31	SW31_P	AR27	SW31_P_PU	AW26
	8	LED32	SW32_P	AG25	SW32_P_PU	AT27

Push Buttons

The DIGILAB SX V features 8 user configurable push buttons. Through an 8-bit three-state DIP switch, the push buttons can be set to be active low, active high or disabled. Furthermore there are programmable pull-up/down resistors for every push button signal. The following diagram shows the functionality of a single push button.

Figure 7: Push Buttons

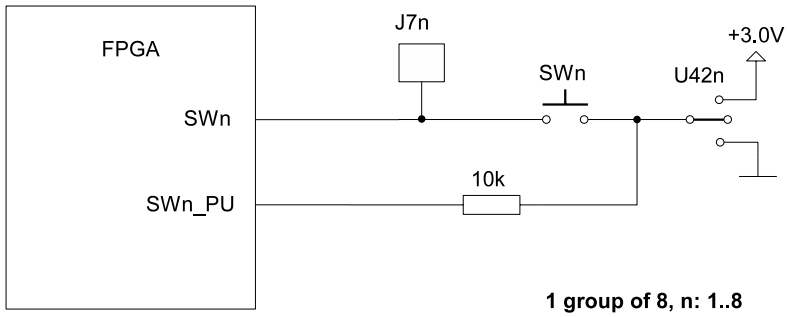

Table 11: Push Buttons

Switch		Signal		Pull-Up/Down Resisotr	
		Name	Stratix V U30 - Pin	Name	Stratix V U30 - Pin
SW	1	SW1	AB25	SW1_PU	AJ24
	2	SW2	AA25	SW2_PU	AG24
	3	SWP	AC25	SW3_PU	AE26
	4	SW4	AC26	SW4_PU	AD26
	5	SW5	AJ26	SW5_PU	AN27
	6	SW6	AK26	SW6_PU	AN26
	7	SW7	AF26	SW7_PU	AM26
	8	SW8	AG26	SW8_PU	AL26

SD/MMC Connector

The DIGILAB SX V features an SD (Secure Digital)/MultiMediaCard (MMC) card connector (U61). This connector can be used to insert standard SD/MMC cards. The SD/MultiMediaCard card is a universal low cost data storage and communication media. It was designed to cover a wide area of applications, such as electronic toys, organizers, PDAs, cameras, smart phones, digital recorders, MP3 players, etc. The SD/MultiMediaCard card communication is based on an advanced 7-pin serial bus. All relevant SD/MMC signals are connected directly to the Stratix V device. On the DIGILAB SX V, SD/Multi Media cards may be used as a flexible, non-volatile and mobile storage media. It is up to the user to create an interface between the SD/MMC card and e.g. a NIOS II or custom logic. Contact El Camino for information on availability of ready to use SD/MMC interfaces, NIOS II library functions and drivers.

Table 12: SD/MMC Connector

SD Card Function		Connector U61 Pin	Stratix V U30	
SD Mode	SPI Mode		Signal	Pin
CD/DAT3	CS	1	MMC_RSV	AB9
CMD	DI	2	MMC_CMD	AE9
CLK	SCLK	5	MMC_CLK	AC10
DAT0	DO	7	MMC_DAT	AD12
DAT1		8	MMC_DAT2	AD9
DAT2		9	MMC9	AB10
WRITE_PROT_FRONT		12	MMC_WP1	AC9
CARD_DETECT		13	MMC_CDET	AB12

Debug Connectors

The DIGILAB SX V has various, different connectors that can be used to connect debugging logic to the board.

There are two 38 pin AMP/Tyco Matched Impedance Connectors (MICTOR) on the board. More information about these connectors can be found at:
URL: www.tycoelectronics.com
Type: 2-5767004-2

On each of these connectors, there are 32 standard Stratix V user IOs in addition to two PLL clock outputs/user IOs .
The signals of MICTOR connector J4 are routed directly to the FPGA and are therefor optimized for high speed. These pins connect to bank 8 of the FPGA which can be switched from 3.0V to 2.5V operation by opening jumper J12. The signals of J5 are also available through standard dual row .100 inch headers (IOs on J24,25,26,27 and clocks on J3/J29) for easy access to individual signals.

The following tables lists the signal names and pin numbers for these connectors.

Table 13: MICTOR connector J5

Header		Stratix V U30 - Pin	Signal	J5		Signal	Stratix V U30 - Pin	Header	
Con.	Pin			Pin	Pin			Pin	Con.
N/A	N/A	N/A	GND	1	38	GND	N/A	N/A	N/A
N/A	N/A	N/A	GND	2	37	GND	N/A	N/A	N/A
J3	1	AC30	LA_CLK0_J5_R	3	36	LA_CLK1_J5_R	AB30	1	J29
J27	1	AN31	LA_A3_7	4	35	LA_A1_7	AP30	1	J24
	3	AT33	LA_A3_6	5	34	LA_A1_6	AJ33	3	
	5	AL33	LA_A3_5	6	33	LA_A1_5	AK33	5	
	7	AH33	LA_A3_4	7	32	LA_A1_4	AK32	7	
	9	AF31	LA_A3_3	8	31	LA_A1_3	AH30	9	
	11	AH31	LA_A3_2	9	30	LA_A1_2	AR30	11	
	13	AG31	LA_A3_1	10	29	LA_A1_1	AE31	13	
	15	AJ32	LA_A3_0	11	28	LA_A1_0	AJ30	15	
J26	1	AU32	LA_A2_7	12	27	LA_A0_7	AT32	1	J25
	3	AM31	LA_A2_6	13	26	LA_A0_6	AR31	3	
	5	AW34	LA_A2_5	14	25	LA_A0_5	AV34	5	
	7	AP31	LA_A2_4	15	24	LA_A0_4	AP33	7	
	9	AV32	LA_A2_3	16	23	LA_A0_3	AU33	9	
	11	AW32	LA_A2_2	17	22	LA_A0_2	AR33	11	
	13	AV31	LA_A2_1	18	21	LA_A0_1	AU34	13	
	15	AW31	LA_A2_0	19	20	LA_A0_0	AU30	15	

Table 14: High-Speed MICTOR connector J4

Stratix V U30 - Pin	Signal	J5		Signal	Stratix V U30 - Pin
		Pin	Pin		
N/A	GND	1	38	GND	N/A
N/A	GND	2	37	GND	N/A
AD30	LA_CLK3_J4	3	36	LA_Q1_CLK_J4	AE30
J25	LA_C1_7	4	35	LA_C3_7	K34
P26	LA_C1_6	5	34	LA_C3_6	J34
N26	LA_C1_5	6	33	LA_C3_5	K33
U25	LA_C1_4	7	32	LA_C3_4	J33
P28	LA_C1_3	8	31	LA_C3_3	G33
K24	LA_C1_2	9	30	LA_C3_2	N33
J26	LA_C1_1	10	29	LA_C3_1	M33
H26	LA_C1_0	11	28	LA_C3_0	U31
M27	LA_C0_7	12	27	LA_C2_7	T31
L27	LA_C0_6	13	26	LA_C2_6	L28
K31	LA_C0_5	14	25	LA_C2_5	K28
J31	LA_C0_4	15	24	LA_C2_4	N28
L31	LA_C0_3	16	23	LA_C2_3	M29
L30	LA_C0_2	17	22	LA_C2_2	R29
R30	LA_C0_1	18	21	LA_C2_1	P29
R31	LA_C0_0	19	20	LA_C2_0	K25

Expansion Connectors

The DIGILAB SX V has various connectors that can be used to connect user logic or custom adapter boards.

There are two 120 pin (J15, J16) as well as one 160 pin (J35) Samtec QSH Hi-Speed connectors on the board. The latter one is based on Altera's HSMC standard.
More information about the connectors can be found on the Samtec website at:
URL: www.samtec.com
Type: QSH-060-.../ASP-122953-01

Details on the pinout of these connectors can be found in the schematics or in the netlist, that is provided with the DIGILAB SX V.

Clocking

The DIGILAB SX V development board includes an 80 MHz oscillator, as well as an 25 MHz oscillator that drive the Stratix V FPGA. In addition there are three SMA clock inputs, feeding comparators, driving into clock buffers. The clock buffers are driving the FPGA and various expansion connectors. The signal length between A, B and C clocks are closely matched in order to provide minimal skew between the individual, external clocks.

The Stratix V FPGA contains multiple phase locked loops (PLLs) and global clock networks for clock management. Stratix V fractional PLLs offer clock multiplication and division, phase shifting, programmable duty cycle, external clock outputs and more, allowing system-level clock management and skew control on the DIGILAB SX V.
The following diagram shows all clock inputs and outputs and how they are connected to the individual PLLs and connectors.

All unused, dual purpose clock inputs are connected to GND on the board. It is important that these pins are either reserved as inputs or reserved as IOs driving ground in the user design.

Figure 8: Clocking Circuitry

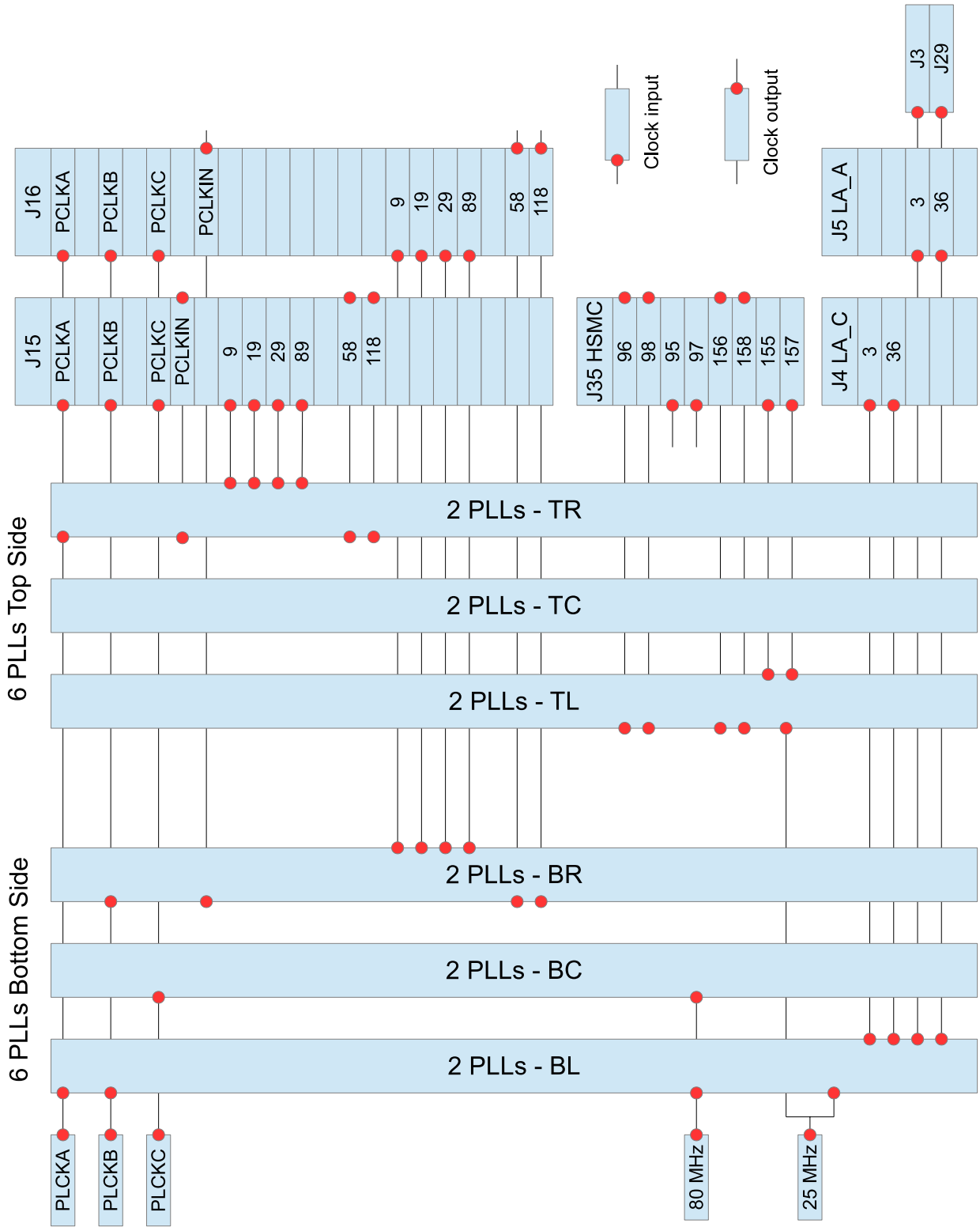

Table 15: Clock Signals

Signal	Dir. at FPGA	Board Connection	Stratix V Clock Signal	PLL	Stratix V Pin
80MHz	IN	oscillator - U5	CLK2P CLK5P	BL BC	AF29 AK23
25MHz_A 25MHz_B	IN	oscillator - U71	CLK21P CLK0P	TL BL	D33 AV29
PCLKA_FPGA	IN	J21(SMA) J15-41 J16-41 PCLKA_FPGA1_LA PCLKA_FPGA1	CLK1P CLK13P	BL TR	AV28 L6
PCLKB_FPGA	IN	J19(SMA) J15-51 J16-51 PCLKB_FPGA1_LA PCLKB_FPGA1	CLK3P CLK9P	BL BR	AG28 AN6
PCLKC_FPGA	IN	J20(SMA) J15-69 J16-69 PCLKC_FPGA1	CLK4P	BC	AH22
PCLKIN_J15	IN	J15-79	CLK12P	TR	G7
PCLKIN_J16	IN	J16-79	CLK11P	BR	AV7
PER1CON_58_CLKIN	IN	J15-58	CLK14P	TR	B7
CLKIN_J15_118	IN	J15-118	CLK15P	TR	D7
PER2CON_58_CLKIN	IN	J16-58	CLK10P	BR	AR8
CLKIN_J16_118	IN	J16-118	CLK8P	BR	AL7
CLKOUT_J15_9	OUT	J15-9	CLKOUT2	TR	A3
CLKOUT_J15_19	OUT	J15-19	CLKOUT3	TR	A4
CLKOUT_J15_29	OUT	J15-29	CLKOUT0	TR	A6
CLKOUT_J15_89	OUT	J15-89	CLKOUT1	TR	A5
CLKOUT_J16_9	OUT	J16-9	CLKOUT0	BR	AT6
CLKOUT_J16_19	OUT	J16-19	CLKOUT1	BR	AU6
CLKOUT_J16_29	OUT	J16-29	CLKOUT3	BR	AR7
CLKOUT_J16_89	OUT	J16-89	CLKOUT2	BR	AP7
MEZ_CLK_IN_P/N	IN	J35-96/98	CLK23P/N	TL	R32/P32
MEZ_CLK2_IN_P/N	IN	J35-156/158	CLK22P/N	TL	N32/M32
MEZ_CLK_OUT_P/N	OUT	J35-95/97	TX122P/N	-	M20/L20
MEZ_CLK2_OUT_P/N	OUT	J35-155/157	CLKOUT0/1	TL	P34/N34
LA_CLK3_J4	OUT	J4-3	CLKOUT0	BL	AD30
LA_Q1_CLK_J4	OUT	J4-36	CLKOUT1	BL	AE30
LA_CLK1_J5	OUT	J5-36, J29-1	CLKOUT2	BL	AB30
LA_CLK0_J5	OUT	J5-3, J3-1	CLKOUT3	BL	AC30

Configuration

The DIGILAB SX V uses an Altera EPCQ512 serial configuration device for non-volatile configuration data storage. The FPGA is setup for Standard Active Serial configuration mode. Upon power-up the DIGILAB SX V will start configuration from address 0x0 of the serial configuration device. A configuration cycle can also be triggered by pushing SW9 (marked as „SW9 Config“) which pulls the nConfig input of the FPGA low.
In addition, the FPGA can be programmed through the JTAG interface.

There is a device errata for the EPCQ device which says that x4 mode is currently not supported. Although the EPCQ is wired in x4 mode on the board, the programming files needs to be generated for x1 mode.

JTAG Connector

J14 is a 10-pin JTAG interface connector compatible with current Altera ByteBlaster, USB-Blaster and Ethernet-Blaster download cables. The JTAG connection can be used for any of the following purposes:

- Quartus II software can configure the Stratix V device (U30) with a new bitstream (such as .sof) file.
- Quartus II can re-program the serial configuration device EPCQ with a JTAG indirect configuration file (.jic)
- The following Altera JTAG accessible functions can be used:
  - SignalTap II Logic Analyzer
  - In-System Memory Content Editor
  - Logic Analyzer Interface Editor
  - In-System Sources and Probes
  - NIOS II Debugging Interface

The JTAG programming interface is not available if the Stratix V has been protected by programming a non-volatile security key.

The JTAG connection is most commonly used to download user configuration files (such as .sof) to the Stratix V device during logic development and debugging.

Notes:

El Camino GmbH
Landshuter Str. 1
D-84048 Mainburg
Germany
Telefone +49-8751-8787-0
Telefax +49-8751-8787-10
E-mail: info@elca.de
http://www.elcamino.de

DIGILAB SX V V1.0

Prel H Stand Proto

Preliminary

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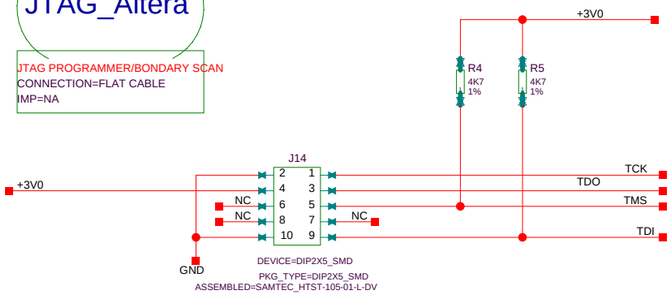
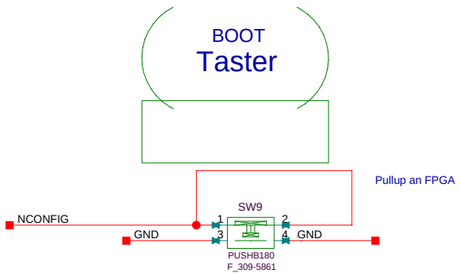
Title	DIGILAB SX V
Document Name	STRATIXV_V1_0
Author	FH
Date	9-15-2014_17:54
Sheet	1

JTAG_Altera

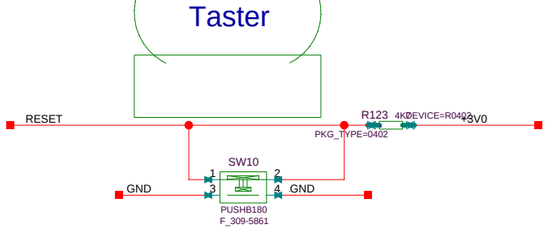
JTAG PROGRAMMER/BONDARY SCAN
CONNECTION=FLAT CABLE
IMP=NA

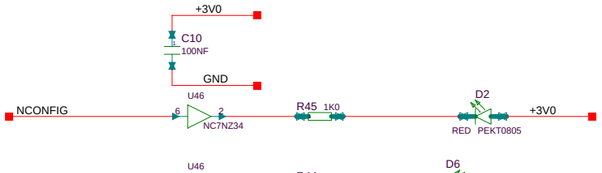


BOOT Taster

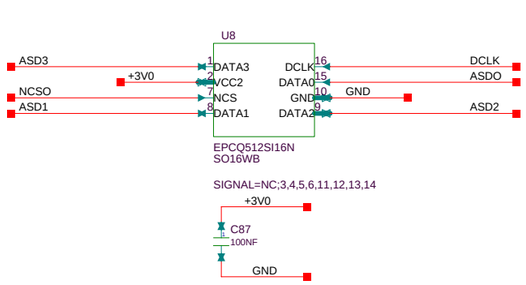


RESET Taster

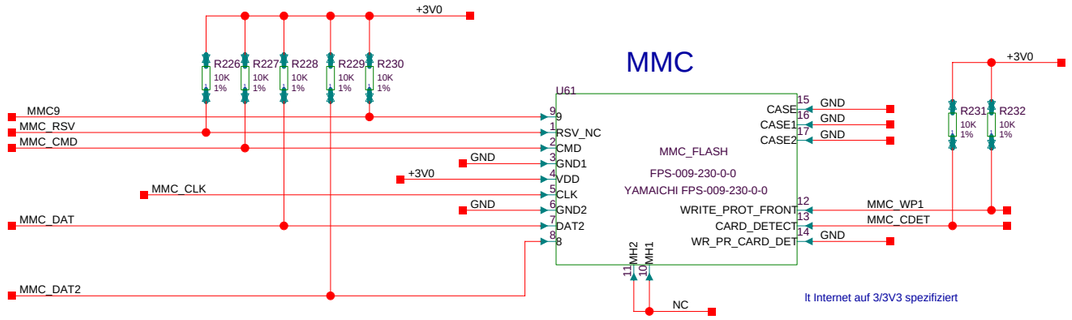




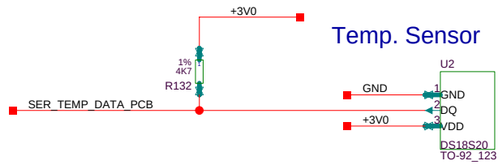
Serial MEM Config



MMC



Temp. Sensor



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Document Name	STRATIXV_V1_0
Author	FH
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Dip Switch LEDs next page

J9 — 2 FPGA Input — SIP-8P
SW1_P
SW2_P
SW3_P
SW4_P
SW5_P
SW6_P
SW7_P
SW8_P

U14
R47 1K0
R48 1K0
R50 1K0
R49 1K0
R56 1K0
R55 1K0
R54 1K0
R53 1K0
AN1 10 GND
AN2 9 +3V0
ETD108ET
ETD108ET
DISTRELEC 210370

FPGA Pullup/Pulldown Select
SW1_P_PU R178 10K
SW2_P_PU R177 10K
SW3_P_PU R176 10K
SW4_P_PU R175 10K
SW5_P_PU R174 10K
SW6_P_PU R173 10K
SW7_P_PU R172 10K
SW8_P_PU R171 10K

J8 — 2 FPGA Input — SIP-8P
SW17_P
SW18_P
SW19_P
SW20_P
SW21_P
SW22_P
SW23_P
SW24_P

U41
R126 1K0
R124 1K0
R120 1K0
R119 1K0
R118 1K0
R117 1K0
R116 1K0
R81 1K0
AN1 10 GND
AN2 9 +3V0
ETD108ET
ETD108ET
DISTRELEC 210370

FPGA Pullup/Pulldown Select
SW17_P_PU R170 10K
SW18_P_PU R169 10K
SW19_P_PU R168 10K
SW20_P_PU R167 10K
SW21_P_PU R166 10K
SW22_P_PU R165 10K
SW23_P_PU R164 10K
SW24_P_PU R163 10K

R204 10K +3V0
R203 10K +3V0
R205 10K +3V0
R206 10K +3V0

J2
SW_SEL1
SW_SEL2
SW_SEL3
SW_SEL4
MK_2X4_90
MULTICOMP MCDP04 F_947-1600
ROHS=OK
GND

R208 10K +3V0
R207 10K +3V0
R209 10K +3V0
R210 10K +3V0

J32
SW_SEL5
SW_SEL6
SW_SEL7
SW_SEL8
MK_2X4_90
MULTICOMP MCDP04 F_947-1600
ROHS=OK
GND

R212 10K +3V0
R211 10K +3V0
R213 10K +3V0
R214 10K +3V0

J33
SW_SEL9
SW_SEL10
SW_SEL11
SW_SEL12
MK_2X4_90
MULTICOMP MCDP04 F_947-1600
ROHS=OK
GND

R216 10K +3V0
R215 10K +3V0
R217 10K +3V0
R218 10K +3V0

J34
SW_SEL13
SW_SEL14
SW_SEL15
SW_SEL16
MK_2X4_90
MULTICOMP MCDP04 F_947-1600
ROHS=OK
GND

J10 — 2 FPGA Input — SIP-8P
SW9_P
SW10_P
SW11_P
SW12_P
SW13_P
SW14_P
SW15_P
SW16_P

U15
R64 1K0
R63 1K0
R62 1K0
R61 1K0
R60 1K0
R59 1K0
R58 1K0
R57 1K0
AN1 10 GND
AN2 9 +3V0
ETD108ET
ETD108ET
DISTRELEC 210370

FPGA Pullup/Pulldown Select
SW9_P_PU R186 10K
SW10_P_PU R185 10K
SW11_P_PU R184 10K
SW12_P_PU R183 10K
SW13_P_PU R182 10K
SW14_P_PU R181 10K
SW15_P_PU R180 10K
SW16_P_PU R179 10K

J11 — 2 FPGA Input — SIP-8P
SW25_P
SW26_P
SW27_P
SW28_P
SW29_P
SW30_P
SW31_P
SW32_P

U40
R72 1K0
R71 1K0
R70 1K0
R69 1K0
R68 1K0
R67 1K0
R66 1K0
R65 1K0
AN1 10 GND
AN2 9 +3V0
ETD108ET
ETD108ET
DISTRELEC 210370

FPGA Pullup/Pulldown Select
SW25_P_PU R194 10K
SW26_P_PU R193 10K
SW27_P_PU R192 10K
SW28_P_PU R191 10K
SW29_P_PU R190 10K
SW30_P_PU R189 10K
SW31_P_PU R188 10K
SW32_P_PU R187 10K

Taster

FPGA Pullup/Pulldown Select
SW4_PU R198 10K
SW3_PU R197 10K
SW2_PU R196 10K
SW1_PU R195 10K

FPGA Pullup/Pulldown Select
SW8_PU R202 10K
SW7_PU R201 10K
SW6_PU R200 10K
SW5_PU R199 10K

SW1 — PUSHB180 F_309-5861
SW2 — PUSHB180 F_309-5861
SW3 — PUSHB180 F_309-5861
SW4 — PUSHB180 F_309-5861
SW5 — PUSHB180 F_309-5861
SW6 — PUSHB180 F_309-5861
SW7 — PUSHB180 F_309-5861
SW8 — PUSHB180 F_309-5861

J7 — SIP-8P

U42
AN1 10 GND
AN2 9 +3V0
ETD108ET
ETD108ET
DISTRELEC 210370

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Author	FH
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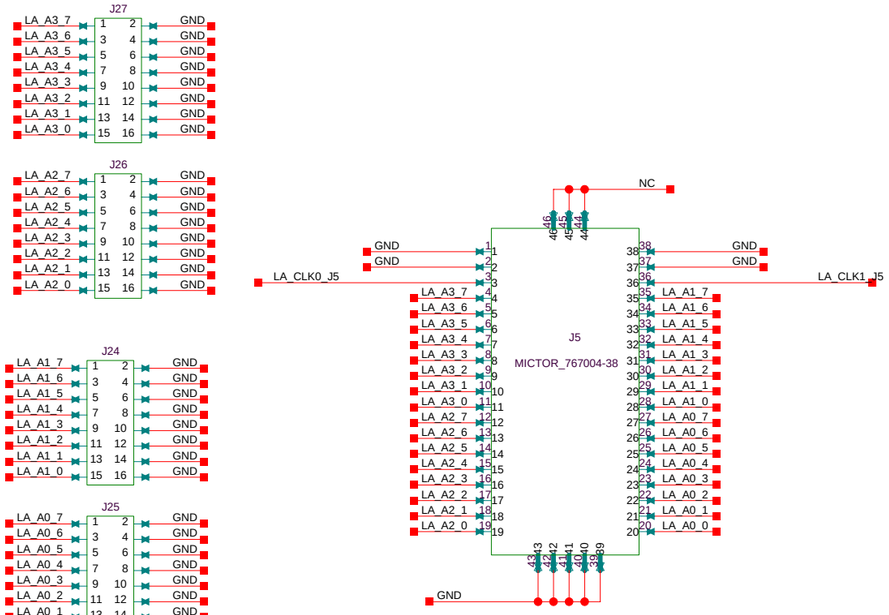
A B C D E F G H I J

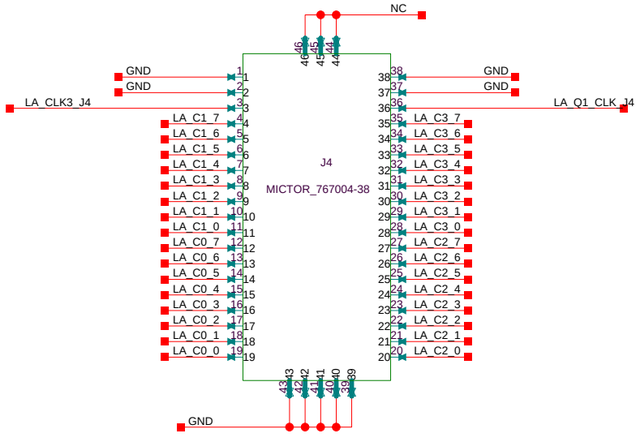
7 6 5 4 3 2 1

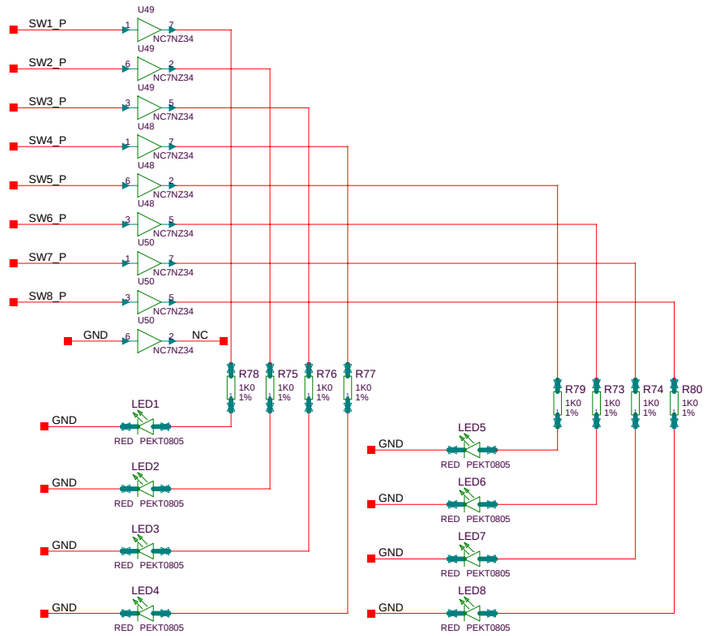
LEDs

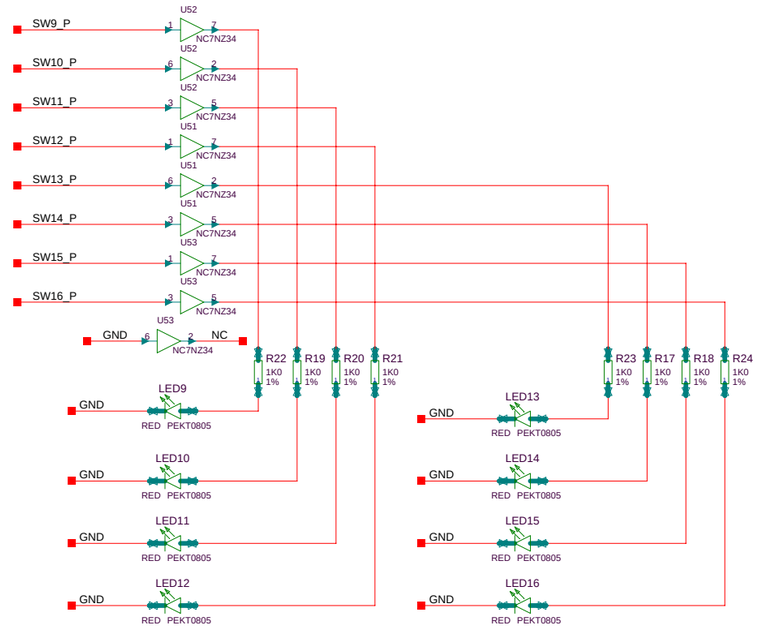
Gen. IO / LA Interface

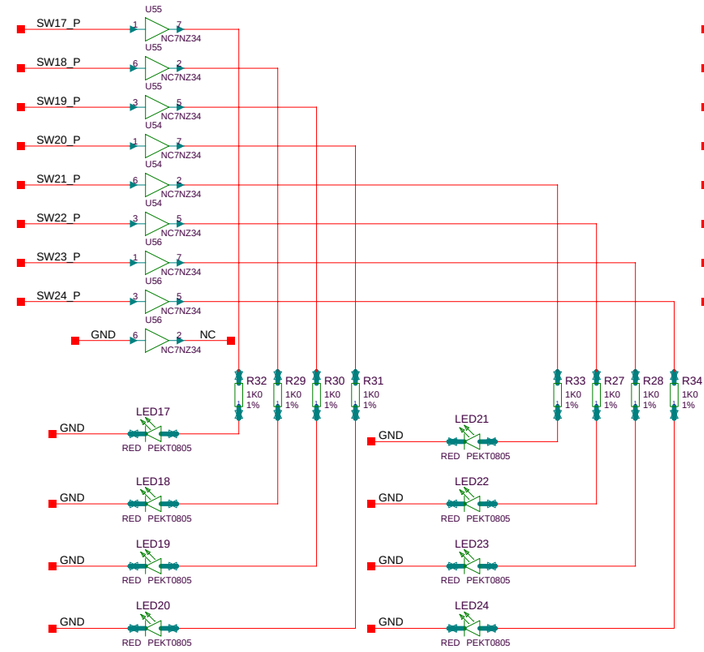


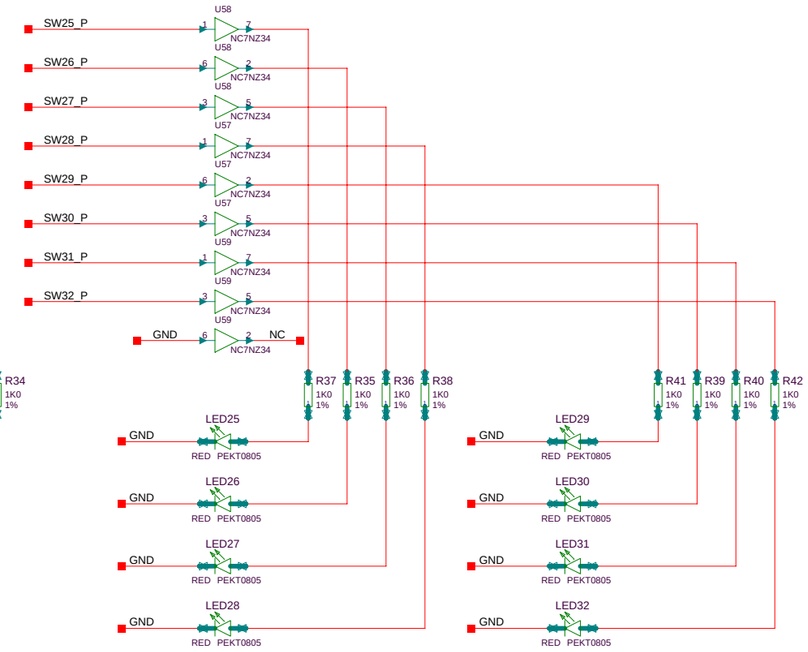
High Speed Gen. IO / LA Interface











Preliminary

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1 2 3 4 5 6 7

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CONNECTION=FLAT CABLE
IMP=NA

SPI

CONNECTION=FLAT CABLE
IMP=NA

RS232_0

CONNECTION=CABLE
RS232

RS232_1

CONNECTION=CABLE
RS232

Power RS232

MAX3238
SSOP28

LP38500SD
LLP8

RJ45_LED
ASSEMBLED_F_I473-9528 / B_73F6730

DIP2X10
DIP2X5

CM1218
SOT23

NC7NZ34

PEKT0805 RED

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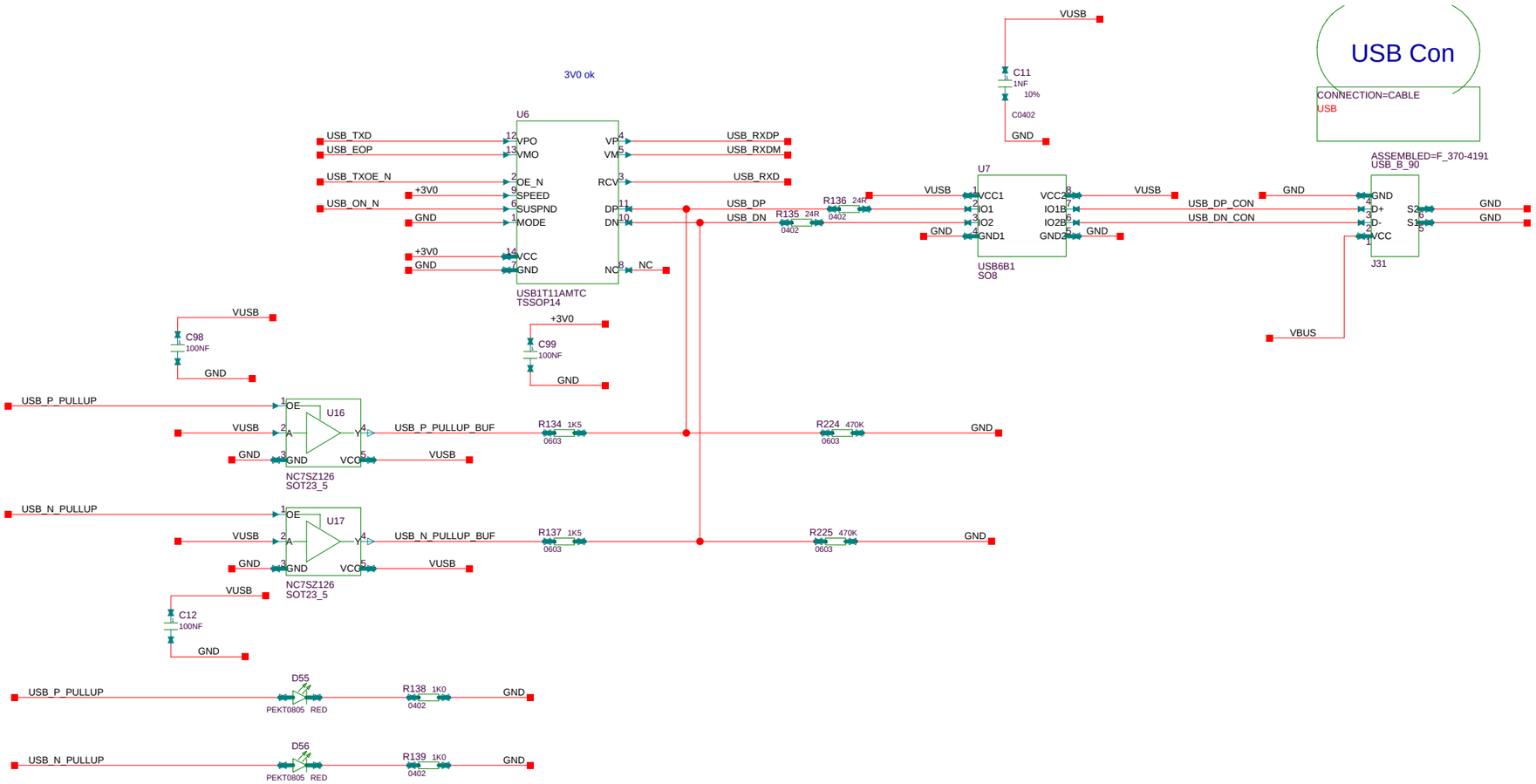
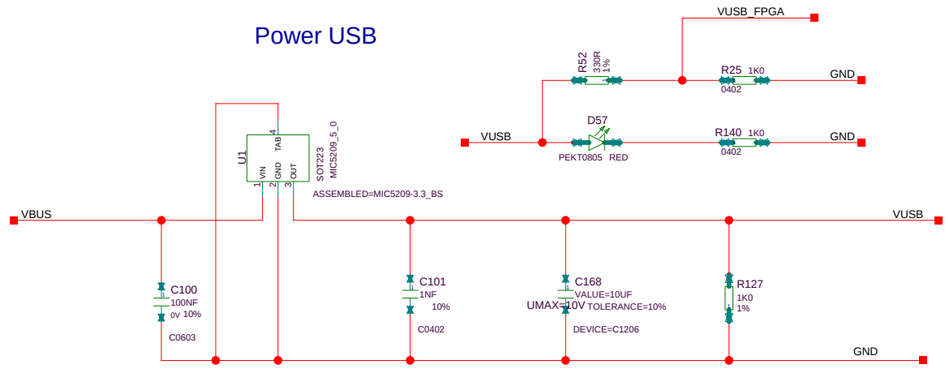
Document Name: STRATIXV_V1_0	Author: FH
Date: 9-15-2014_8:31	Sheet: 5



Power USB



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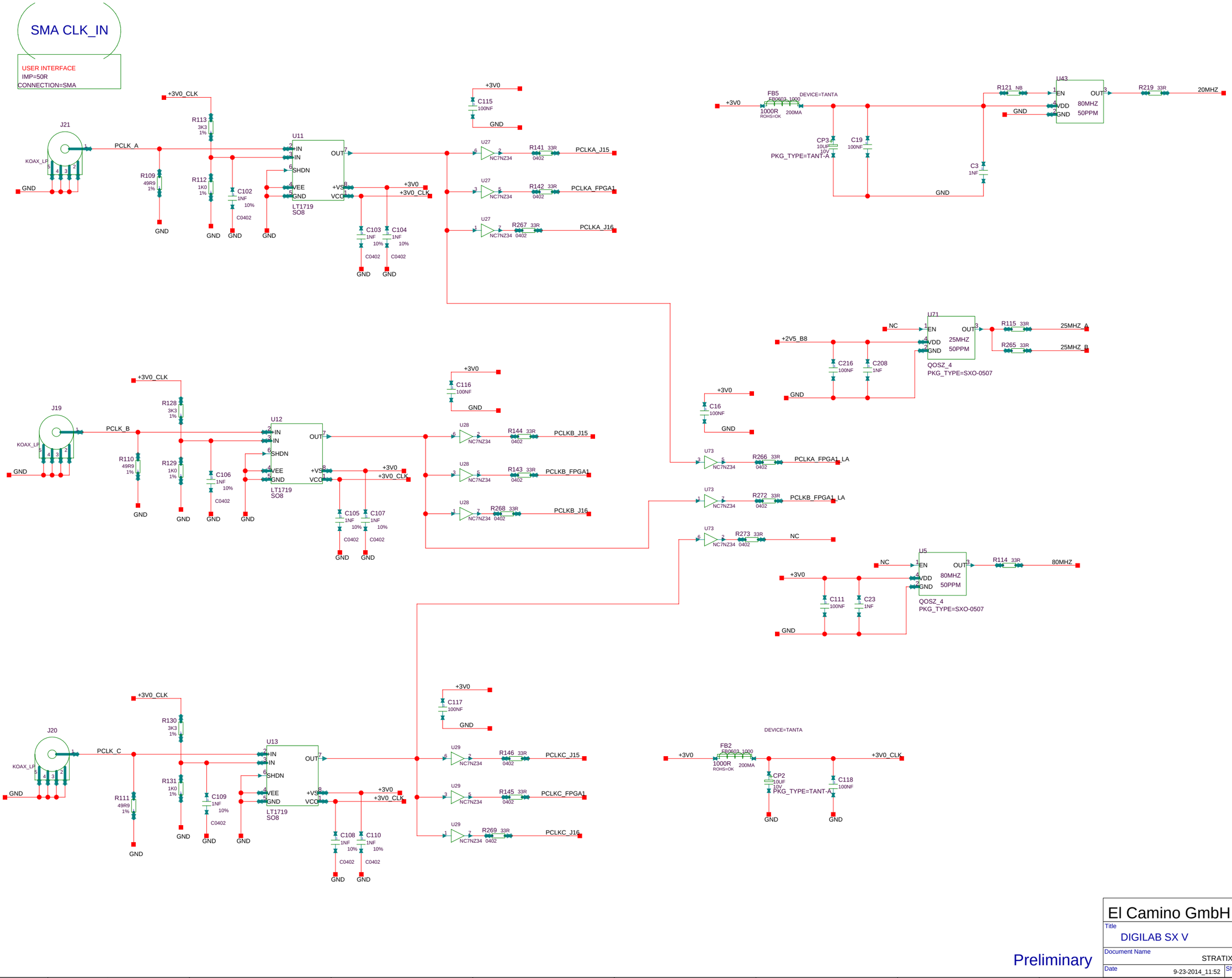
Sheet	6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USER INTERFACE
IMP=50R
CONNECTION=SMA
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KOAX_LF
PCLK_A
+3V0_CLK
R113 3K3 1%
R109 49R9 1%
R112 1K0 1%
C102 1NF 10%
C0402
U11
+IN
-IN
SHDN
VEE
GND
OUT
+VS
VCC
LT1719
SO8
C115 100NF
+3V0
GND
C103 1NF 10%
C104 1NF 10%
U27
NC7NZ34
R141 33R 0402
R142 33R 0402
R267 33R 0402
PCLKA_J15
PCLKA_FPGA1
PCLKA_J16
FB5 FB0603_1000 DEVICE=TANTA
1000R ROHS=OK
200MA
CP3 10UF 10V
PKG_TYPE=TANT-A
C19 100NF
C3 1NF
R121 NB
R219 33R
20MHZ
U43
EN
VDD
GND
OUT
80MHZ
50PPM
J19
PCLK_B
R128 3K3 1%
R110 49R9 1%
R129 1K0 1%
C106 1NF 10%
U12
C116 100NF
R144 33R 0402
R143 33R 0402
R268 33R 0402
PCLKB_J15
PCLKB_FPGA1
PCLKB_J16
C105 1NF 10%
C107 1NF 10%
U71
NC
25MHZ
QOSZ_4
PKG_TYPE=SXO-0507
R115 33R
R265 33R
25MHZ_A
25MHZ_B
+2V5_B8
C216 100NF
C208 1NF
C16 100NF
U73
R266 33R 0402
R272 33R 0402
R273 33R 0402
PCLKA_FPGA1_LA
PCLKB_FPGA1_LA
NC
U5
80MHZ
50PPM
R114 33R
C111 100NF
C23 1NF
J20
PCLK_C
R130 3K3 1%
R111 49R9 1%
R131 1K0 1%
C109 1NF 10%
U13
C117 100NF
R146 33R 0402
R145 33R 0402
R269 33R 0402
PCLKC_J15
PCLKC_FPGA1
PCLKC_J16
C108 1NF 10%
C110 1NF 10%
FB2 FB0603_1000 DEVICE=TANTA
CP2 10UF 10V
C118 100NF
Preliminary
El Camino GmbH
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DIGILAB SX V
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Author
FH
Date
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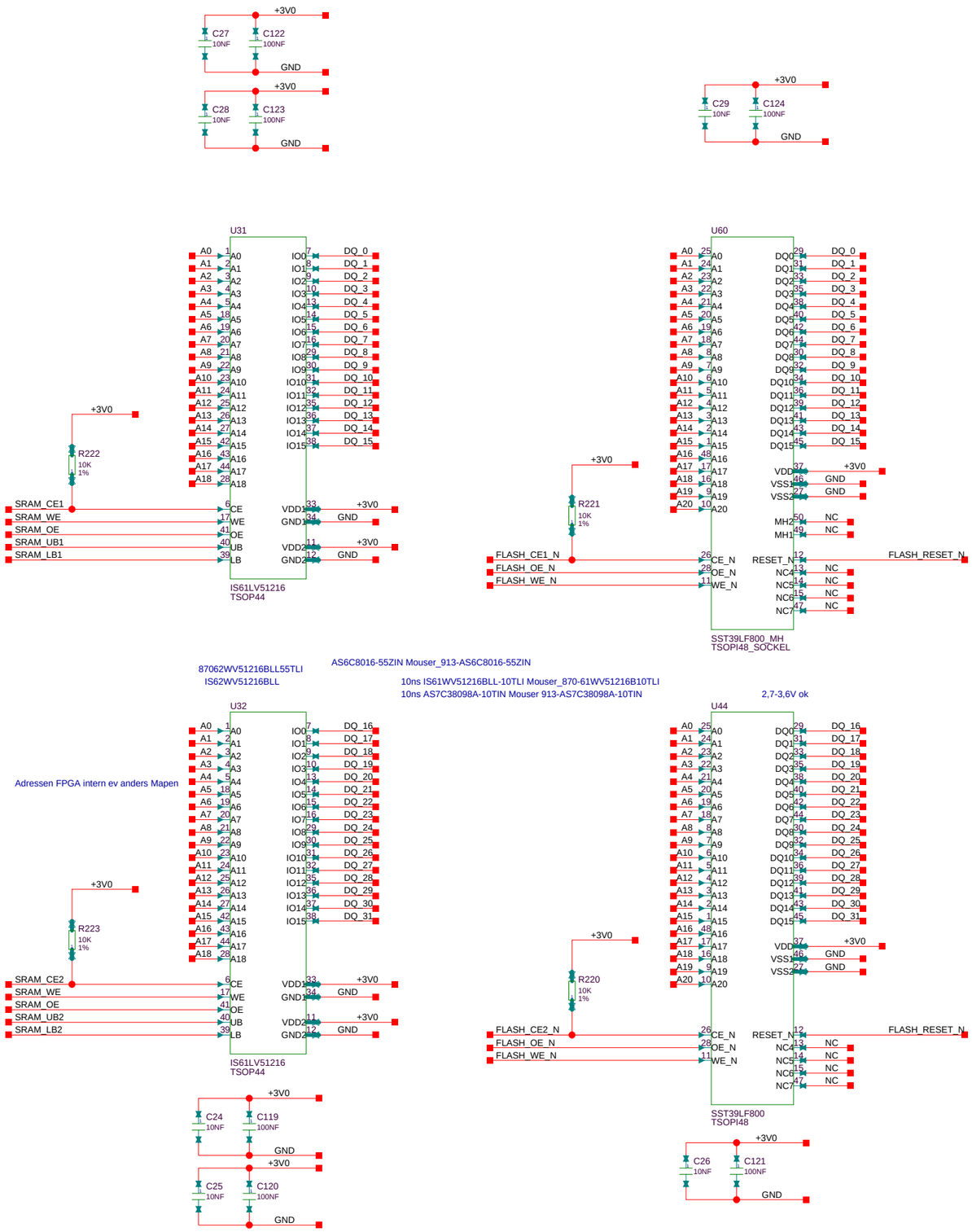

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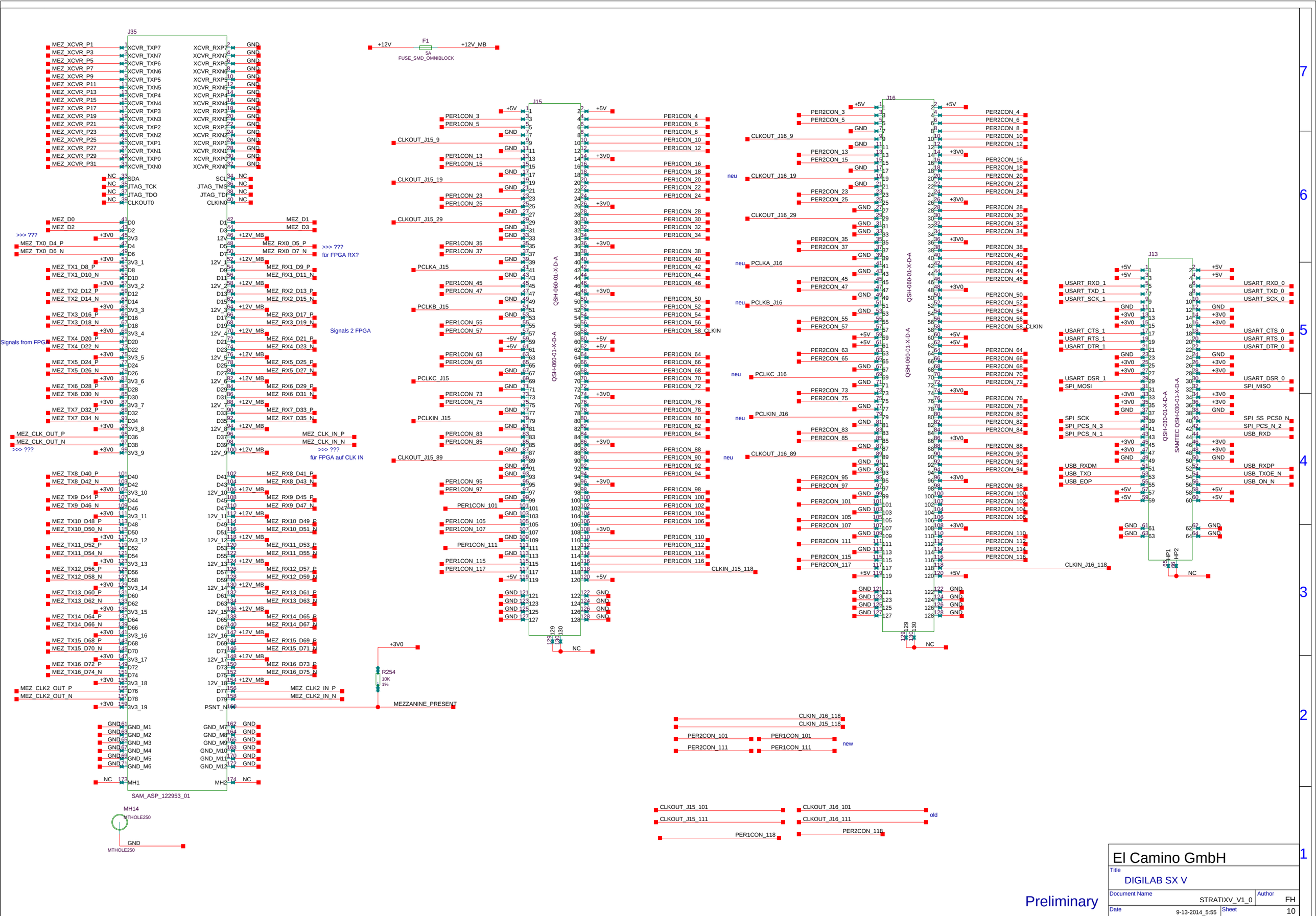
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MEZ_XCVR_P7
MEZ_XCVR_P9
MEZ_XCVR_P11
MEZ_XCVR_P13
MEZ_XCVR_P15
MEZ_XCVR_P17
MEZ_XCVR_P19
MEZ_XCVR_P21
MEZ_XCVR_P23
MEZ_XCVR_P25
MEZ_XCVR_P27
MEZ_XCVR_P29
MEZ_XCVR_P31
XCVR_TXP7
XCVR_TXN7
XCVR_TXP6
XCVR_TXN6
XCVR_TXP5
XCVR_TXN5
XCVR_TXP4
XCVR_TXN4
XCVR_TXP3
XCVR_TXN3
XCVR_TXP2
XCVR_TXN2
XCVR_TXP1
XCVR_TXN1
XCVR_TXP0
XCVR_TXN0
XCVR_RXP7
XCVR_RXN7
XCVR_RXP6
XCVR_RXN6
XCVR_RXP5
XCVR_RXN5
XCVR_RXP4
XCVR_RXN4
XCVR_RXP3
XCVR_RXN3
XCVR_RXP2
XCVR_RXN2
XCVR_RXP1
XCVR_RXN1
XCVR_RXP0
XCVR_RXN0
GND
NC
SDA
SCL
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
CLKOUT0
CLKIN0
MEZ_D0
MEZ_D1
MEZ_D2
MEZ_D3
+3V0
+12V_MB
>>> ???
MEZ_TX0_D4_P
MEZ_TX0_D6_N
MEZ_RX0_D5_P
MEZ_RX0_D7_N
für FPGA RX?
MEZ_TX1_D8_P
MEZ_TX1_D10_N
MEZ_RX1_D9_P
MEZ_RX1_D11_N
MEZ_TX2_D12_P
MEZ_TX2_D14_N
MEZ_RX2_D13_P
MEZ_RX2_D15_N
MEZ_TX3_D16_P
MEZ_TX3_D18_N
MEZ_RX3_D17_P
MEZ_RX3_D19_N
Signals from FPGA
Signals 2 FPGA
MEZ_TX4_D20_P
MEZ_TX4_D22_N
MEZ_RX4_D21_P
MEZ_RX4_D23_N
MEZ_TX5_D24_P
MEZ_TX5_D26_N
MEZ_RX5_D25_P
MEZ_RX5_D27_N
MEZ_TX6_D28_P
MEZ_TX6_D30_N
MEZ_RX6_D29_P
MEZ_RX6_D31_N
MEZ_TX7_D32_P
MEZ_TX7_D34_N
MEZ_RX7_D33_P
MEZ_RX7_D35_N
MEZ_CLK_OUT_P
MEZ_CLK_OUT_N
MEZ_CLK_IN_P
MEZ_CLK_IN_N
>>> ???
für FPGA auf CLK IN
MEZ_TX8_D40_P
MEZ_TX8_D42_N
MEZ_RX8_D41_P
MEZ_RX8_D43_N
MEZ_TX9_D44_P
MEZ_TX9_D46_N
MEZ_RX9_D45_P
MEZ_RX9_D47_N
MEZ_TX10_D48_P
MEZ_TX10_D50_N
MEZ_RX10_D49_P
MEZ_RX10_D51_N
MEZ_TX11_D52_P
MEZ_TX11_D54_N
MEZ_RX11_D53_P
MEZ_RX11_D55_N
MEZ_TX12_D56_P
MEZ_TX12_D58_N
MEZ_RX12_D57_P
MEZ_RX12_D59_N
MEZ_TX13_D60_P
MEZ_TX13_D62_N
MEZ_RX13_D61_P
MEZ_RX13_D63_N
MEZ_TX14_D64_P
MEZ_TX14_D66_N
MEZ_RX14_D65_P
MEZ_RX14_D67_N
MEZ_TX15_D68_P
MEZ_TX15_D70_N
MEZ_RX15_D69_P
MEZ_RX15_D71_N
MEZ_TX16_D72_P
MEZ_TX16_D74_N
MEZ_RX16_D73_P
MEZ_RX16_D75_N
MEZ_CLK2_OUT_P
MEZ_CLK2_OUT_N
MEZ_CLK2_IN_P
MEZ_CLK2_IN_N
PSNT_N
MEZZANINE_PRESENT
R254
10K
1%
3V3_1
3V3_2
3V3_3
3V3_4
3V3_5
3V3_6
3V3_7
3V3_8
3V3_9
3V3_10
3V3_11
3V3_12
3V3_13
3V3_14
3V3_15
3V3_16
3V3_17
3V3_18
3V3_19
GND_M1
GND_M2
GND_M3
GND_M4
GND_M5
GND_M6
GND_M7
GND_M8
GND_M9
GND_M10
GND_M11
GND_M12
MH1
MH2
SAM_ASP_122953_01
MH14
MTHOLE250
F1
5A
FUSE_SMD_OMNIBLOCK
+12V
+12V_MB
J15
QSH-060-01-X-D-A
PER1CON_3
PER1CON_5
CLKOUT_J15_9
PER1CON_13
PER1CON_15
CLKOUT_J15_19
PER1CON_23
PER1CON_25
CLKOUT_J15_29
PER1CON_35
PER1CON_37
PCLKA_J15
PER1CON_45
PER1CON_47
PCLKB_J15
PER1CON_55
PER1CON_57
PCLKC_J15
PER1CON_63
PER1CON_65
PCLKIN_J15
PER1CON_73
PER1CON_75
CLKOUT_J15_89
PER1CON_83
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PER1CON_95
PER1CON_97
PER1CON_101
PER1CON_105
PER1CON_107
PER1CON_111
PER1CON_115
PER1CON_117
CLKIN_J15_118
PER1CON_4
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PER1CON_42
PER1CON_44
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PER1CON_54
PER1CON_56
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PER1CON_68
PER1CON_70
PER1CON_72
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PER1CON_78
PER1CON_80
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PER1CON_102
PER1CON_104
PER1CON_106
PER1CON_110
PER1CON_112
PER1CON_114
PER1CON_116
J16
QSH-060-01-X-D-A
neu
PER2CON_3
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CLKOUT_J16_9
PER2CON_13
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CLKOUT_J16_19
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CLKOUT_J16_29
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PCLKB_J16
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PER2CON_110
PER2CON_112
PER2CON_114
PER2CON_116
J13
SAMTEC QSH-030-01-X-D-A
USART_RXD_1
USART_TXD_1
USART_SCK_1
USART_CTS_1
USART_RTS_1
USART_DTR_1
USART_DSR_1
SPI_MOSI
SPI_SCK
SPI_PCS_N_3
SPI_PCS_N_1
USB_RXDM
USB_TXD
USB_EOP
USART_RXD_0
USART_TXD_0
USART_SCK_0
USART_CTS_0
USART_RTS_0
USART_DTR_0
USART_DSR_0
SPI_MISO
SPI_SS_PCS0_N
SPI_PCS_N_2
USB_RXD
USB_RXDP
USB_TXOE_N
USB_ON_N
HP1
HP2
CLKIN_J16_118
CLKIN_J15_118
PER2CON_101
PER1CON_101
PER2CON_111
PER1CON_111
new
CLKOUT_J15_101
CLKOUT_J15_111
PER1CON_118
CLKOUT_J16_101
CLKOUT_J16_111
PER2CON_118
old
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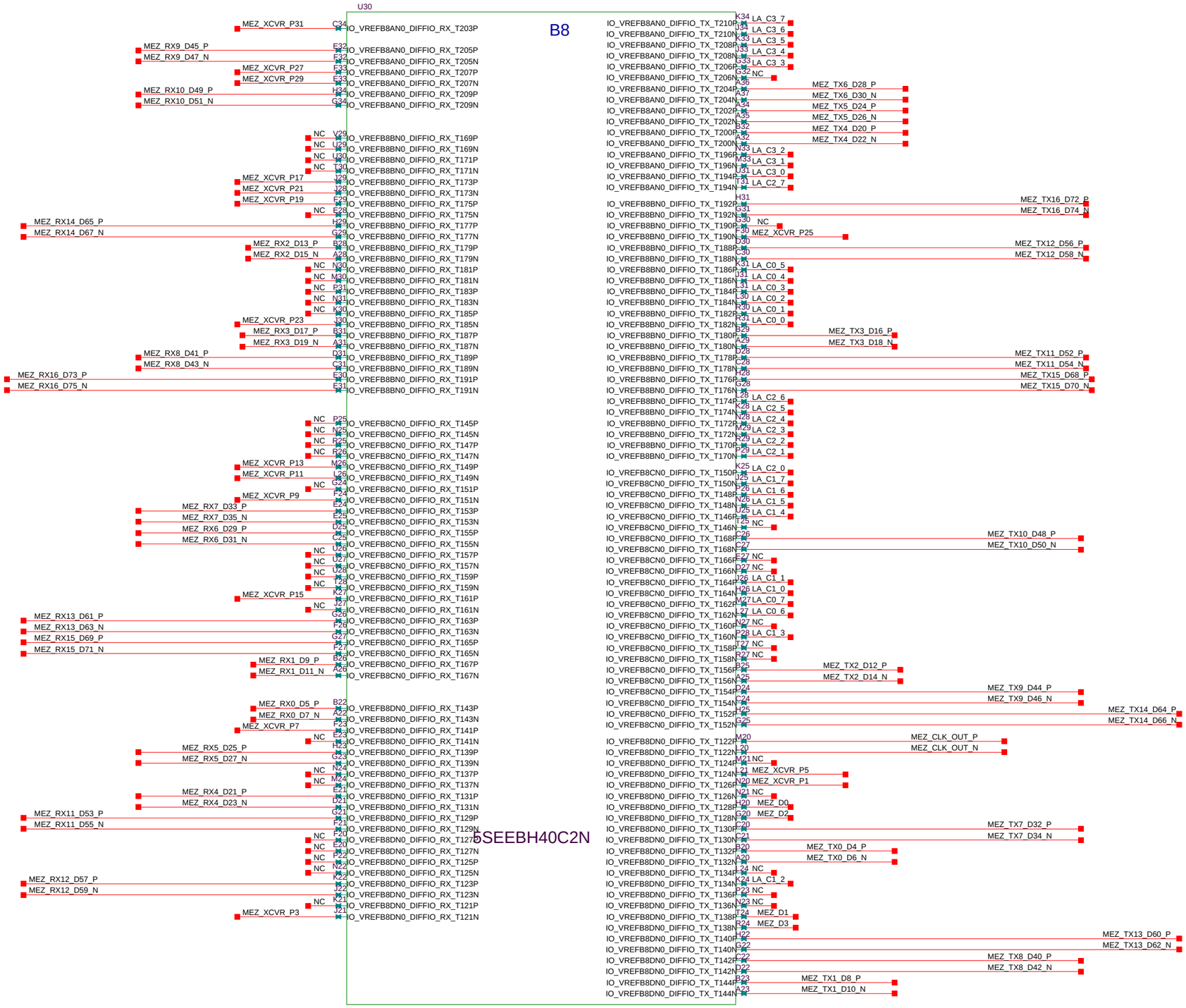
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MEZ_RX9_D45_P
MEZ_RX9_D47_N
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MEZ_RX10_D49_P
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MEZ_RX11_D55_N
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LA_C3_5
LA_C3_4
LA_C3_3
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LA_C3_1
LA_C3_0
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MEZ_XCVR_P25
MEZ_TX12_D56_P
MEZ_TX12_D58_N
LA_C0_5
LA_C0_4
LA_C0_3
LA_C0_2
LA_C0_1
LA_C0_0
MEZ_TX3_D16_P
MEZ_TX3_D18_N
MEZ_TX11_D52_P
MEZ_TX11_D54_N
MEZ_TX15_D68_P
MEZ_TX15_D70_N
LA_C2_6
LA_C2_5
LA_C2_4
LA_C2_3
LA_C2_2
LA_C2_1
LA_C2_0
LA_C1_7
LA_C1_6
LA_C1_5
LA_C1_4
MEZ_TX10_D48_P
MEZ_TX10_D50_N
LA_C1_1
LA_C1_0
LA_C0_7
LA_C0_6
LA_C1_3
MEZ_TX2_D12_P
MEZ_TX2_D14_N
MEZ_TX9_D44_P
MEZ_TX9_D46_N
MEZ_TX14_D64_P
MEZ_TX14_D66_N
MEZ_CLK_OUT_P
MEZ_CLK_OUT_N
MEZ_XCVR_P5
MEZ_XCVR_P1
MEZ_D0
MEZ_D2
MEZ_TX7_D32_P
MEZ_TX7_D34_N
MEZ_TX0_D4_P
MEZ_TX0_D6_N
LA_C1_2
MEZ_D1
MEZ_D3
MEZ_TX13_D60_P
MEZ_TX13_D62_N
MEZ_TX8_D40_P
MEZ_TX8_D42_N
MEZ_TX1_D8_P
MEZ_TX1_D10_N
May be switched to B8
Preliminary
El Camino GmbH
Title
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FH
Date
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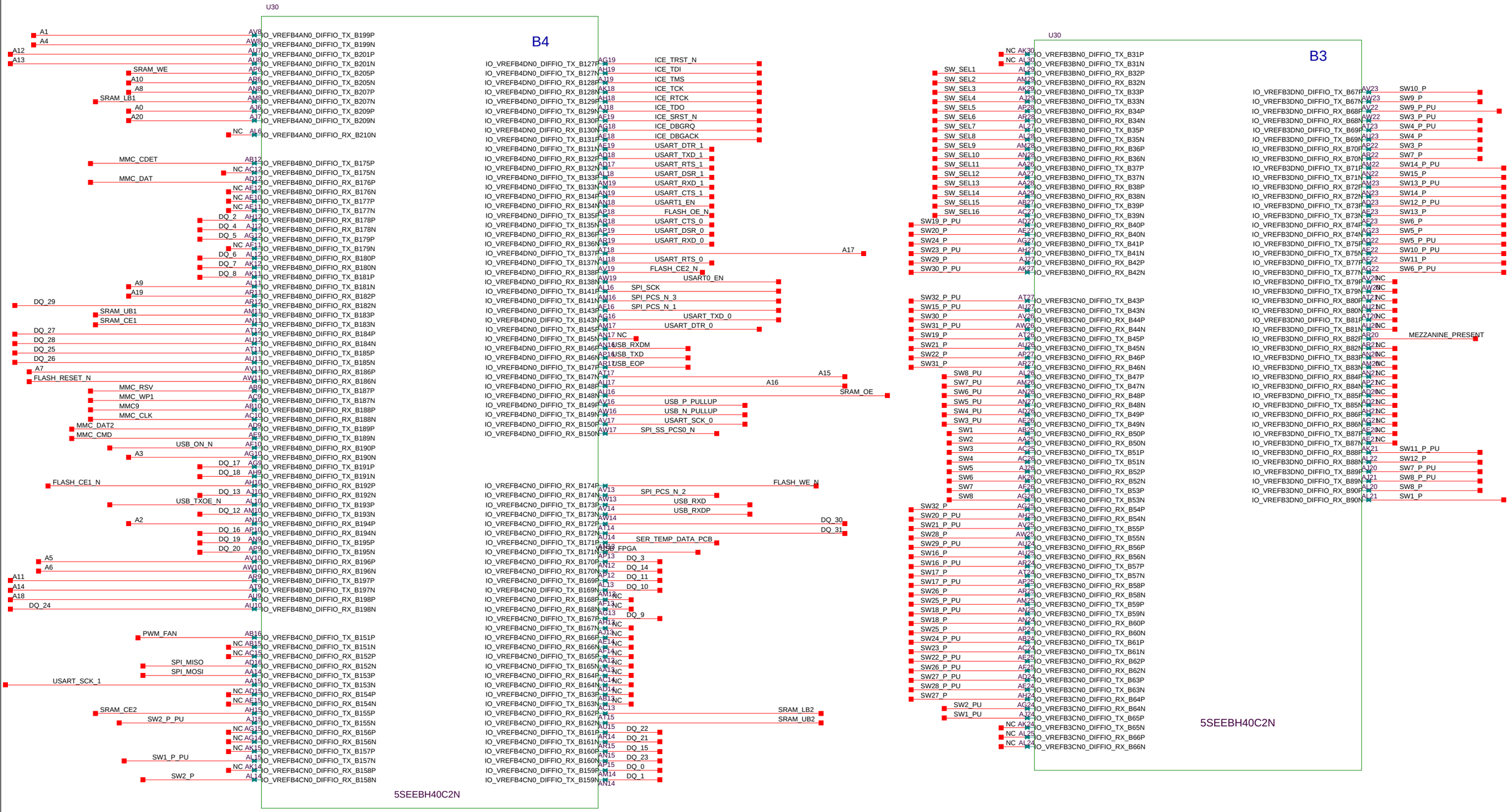
11



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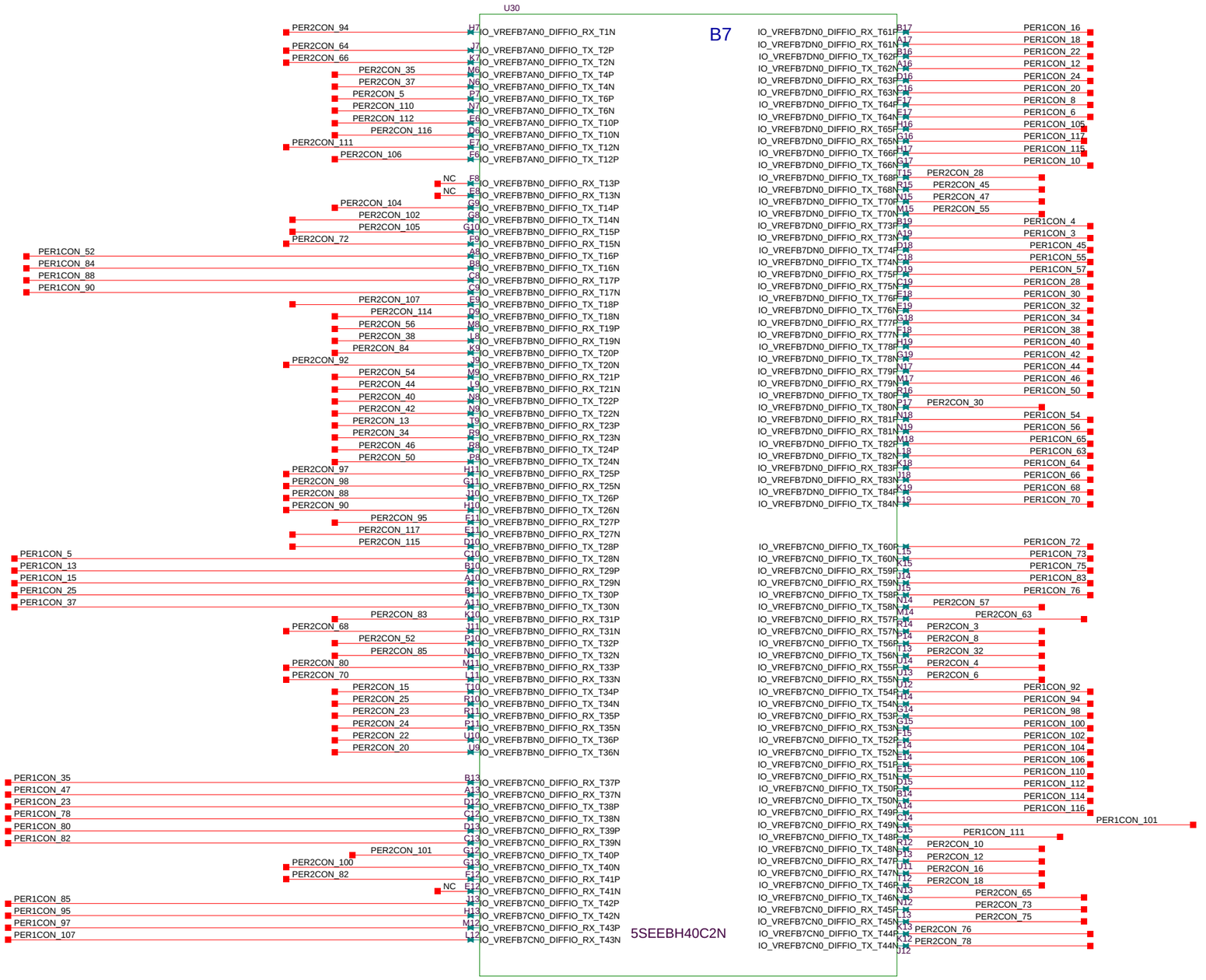

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U30

5SEEBH40C2N

U30

VCC

PU 1

PU 3

PU 2

PU 2

PU 3

PU 2

5SEEBH40C2N

U30

VCCIO

PU 2

5SEEBH40C2N

if NU GND or VCC

config

Preliminary

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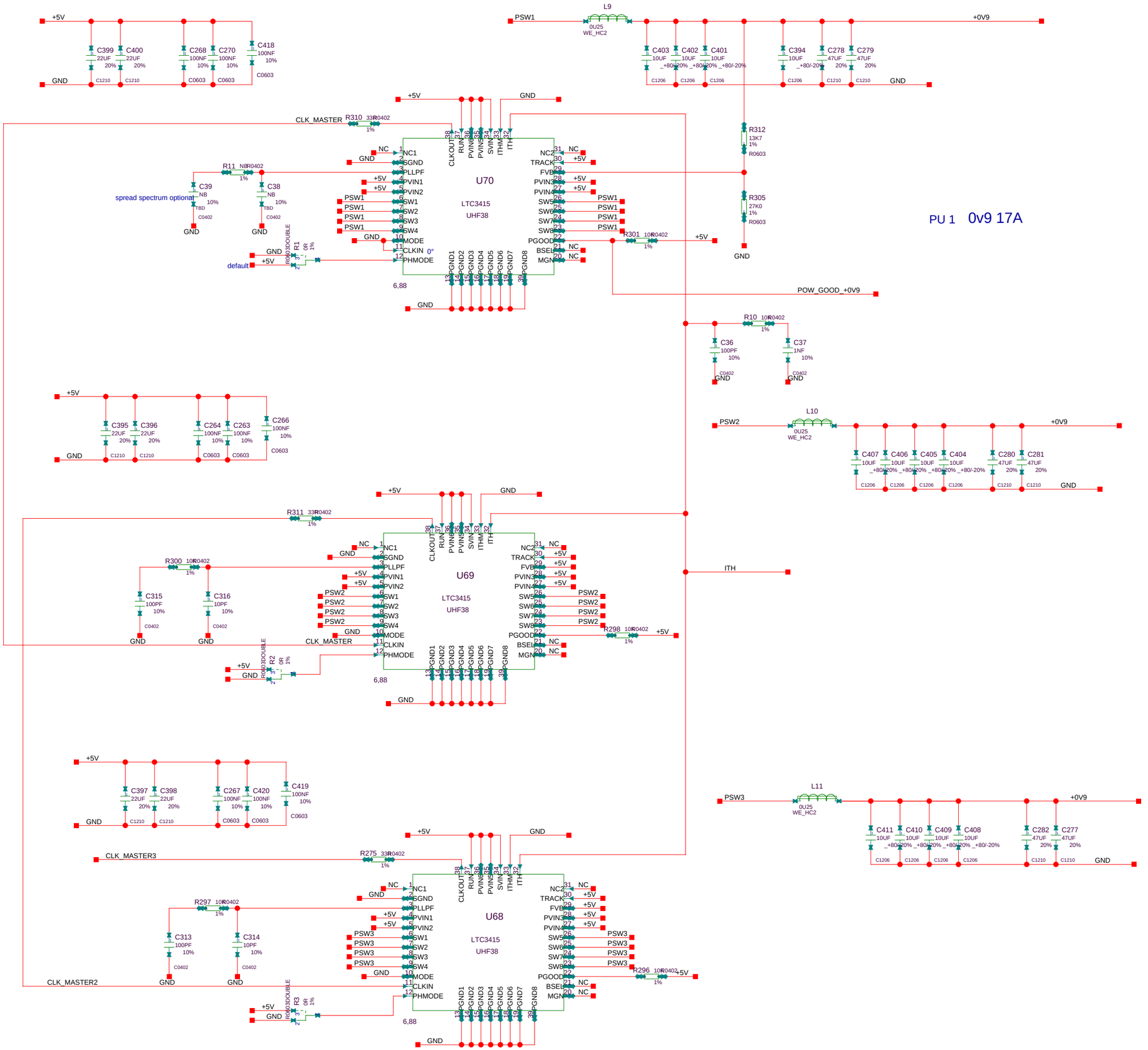

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Messpunkte

+3V0 TP12
+2V5 TP9
+0V9 TP10
+5V TP11
+1V5 TP1
+2V5_B8 TP2
+3V3 TP13
GND TP8
GND TP6
GND TP5
GND TP4
GND TP3
GND TP7

+3V0

+3V0 → R162 10K0 1% R0603 default ON
+5V → R161 1K0 1% R0603 → PWM_FAN
U47 TPS62040L
VIN (4), ON/OFF (5), GND (6), VOUT1_C1 (3), VOUT2_C1 (2), R1_C1 (1), R2
DEVICE=FDC6330L
PKG_TYPE=SUPSOT-6
C13 1NF 10% C0402
R160 100R R0402 1%
GND
D7 SOD80C BAS85 ASSEMBLED=B_10 S 7488 VERS T/R OK (2 → 1)
GND → J30 SIP-2P NA

FAN
USER INTERFACE
IMP=NA
CONNECTION=NO CON

+5V → C169 22UF 20% C1210, C170 22UF 20% C1210, C172 22UF 20% C1210, C173 22UF 20% C1210 → GND

PU 2

PSW4 → L6 0U25 WE_HC2 → +3V0
C237 10UF _+80/-20% C1206, C236 10UF _+80/-20% C1206, C235 10UF _+80/-20% C1206, C234 10UF _+80/-20% C1206
C217 47UF 20% C1210, C218 47UF 20% C1210 → GND

+5V → C228 22UF 20% C1210, C227 22UF 20% C1210
C233 100NF 10% PKG_TYPE=0603 C0603, C231 100NF 10% PKG_TYPE=0603 C0603, C232 100NF 10% PKG_TYPE=0603 C0603 → GND

POW_GOOD_+0V9
+5V → U74 LTC3415 UHF38
CLKOUT (38), RUN (37), PVIN1 (36), PVIN2 (35), SVIN (34), ITHM (33), ITH (32)
NC (1), GND (2), PLLPF (3), PVIN1 (4), PVIN2 (5), SW1 (6), SW2 (7), SW3 (8), SW4 (9), MODE (10), CLKIN (11), PHMODE (12)
NC (31), TRACK (30), FVB (29), PVIN3 (28), PVIN4 (27), SW5 (26), SW6 (25), SW7 (24), SW8 (23), PGOOD (22), BSEL (21), MGN (20)
PGND1 (13), PGND2 (14), PGND3 (15), PGND4 (17), PGND5 (18), PGND6 (19), PGND7 (40), PGND8 (39)
PSW4 ×4, +5V ×2, NC ×2, +5V ×2
R276 100R R0402 1%, C230 100PF 10% C0402, C229 10PF 10% C0402
CLK_MASTER3
R274 0R DOUBLE R0603
6,88
R277 100R R0402 1% → +3V0
POW_GOOD_3V3
R286 27K0 1% R0603, R278 6K8 1% R0603 → GND

Montagebohrungen

MH6 MTHOLE250 GND MTHOLE250, MH5 MTHOLE250 GND MTHOLE250
MH4 MTHOLE250 GND MTHOLE250, MH3 MTHOLE250 GND MTHOLE250
MH2 MTHOLE250 GND MTHOLE250, MH1 MTHOLE250 GND MTHOLE250
MH8 MTHOLE250 GND MTHOLE250, MH7 MTHOLE250 GND MTHOLE250
MH11 MTHOLE250 GND MTHOLE250, MH12 MTHOLE250 GND MTHOLE250
MH10 MTHOLE250 GND MTHOLE250, MH9 MTHOLE250 GND MTHOLE250

+2V5 0,5A

PU 2

U67 PVSON10
+5V → VIN1 (2), VIN2 (3)
POW_GOOD_+0V9 → EN (1)
SW1 (8), SW2 (7) → L2 7U4 L_SRR6038 → +2V5
FB (5) → R261 49K9 1% R0603, C197 270PF 50V C0402
MODE (6) → POS 1-3 R51 0R
GND (4)
PGND1 (10), PGND2 (9), PPAD (11)
C190 10UF 10V C0805, C200 100NF 50V C0603
C189 10UF 10V C0805, C186 10UF 10V C0805, C167 10UF 10V C0805, C171 10UF 10V C0805
R256 12K5 1% R0603, C201 1N5 50V C0603
GND

1V5 900mA

PU 3

U9 TPS62140 PVQFN16
+5V → PVIN1 (11), PVIN2 (12)
POW_GOOD_3V3 → EN (13)
AVIN (10), SS_TR (9), VOS (14), PG (4), FB (5)
SW1 (1), SW2 (2), SW3 (3) → L3 3U3 WE-PD → +1V5
DEF (8), FSW (7)
AGND (6), PGND1 (15), PGND2 (16), PPAD (17)
R7 10K
R255 8K7 1% R0603, R122 10K0 1% R0603
C166 10UF 10V C0805, C199 100NF 50V C0603, C196 1NF
C49 10UF 10V C0805, C48 10UF 10V C0805, C14 10UF 10V C0805, C15 10UF 10V C0805
R26 0R → GND

Passermarken

NC
PM4 FIDUCIAL_RND, PM2 FIDUCIAL_RND
PM3 FIDUCIAL_RND, PM1 FIDUCIAL_RND

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A B C D E F G H I J
7 6 5 4 3 2 1

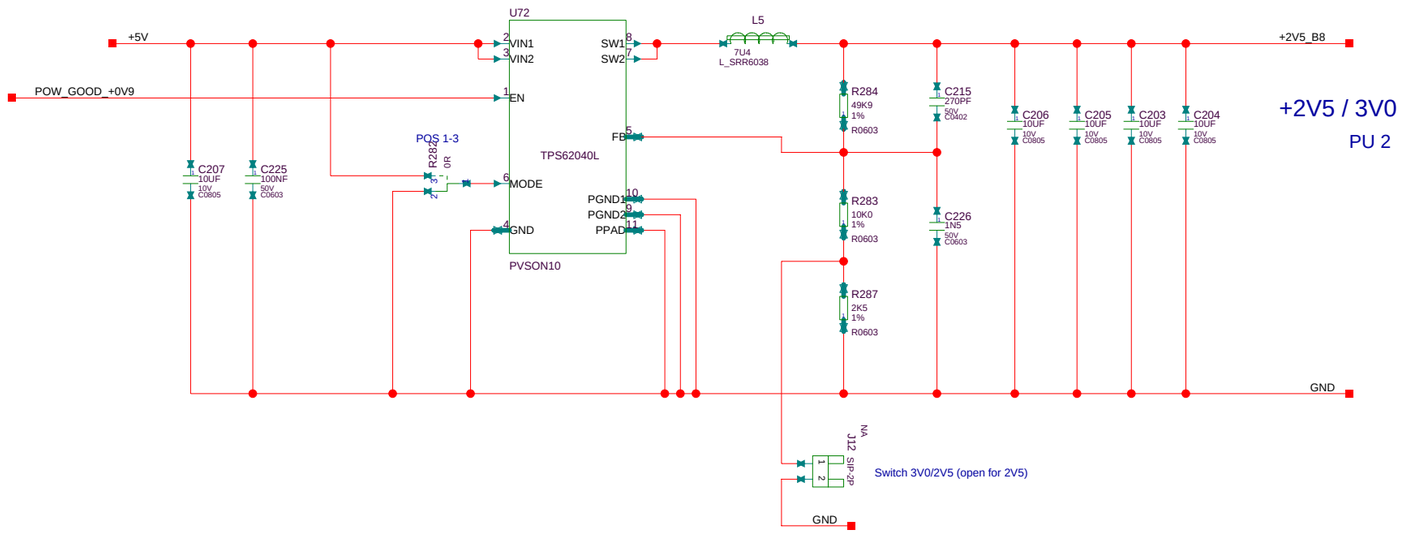
POWER PLUGs

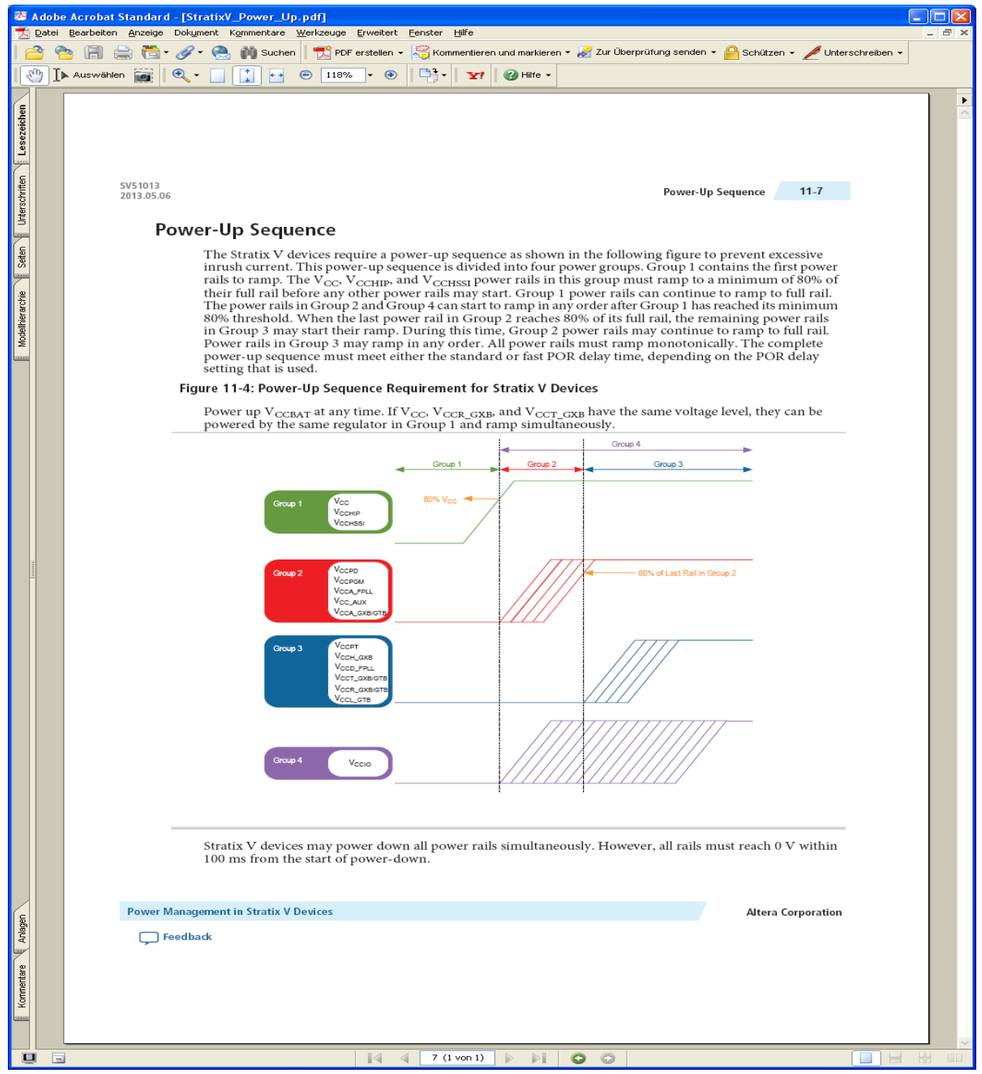
USER INTERFACE
IMP=NA
CONNECTION=FLOPPY

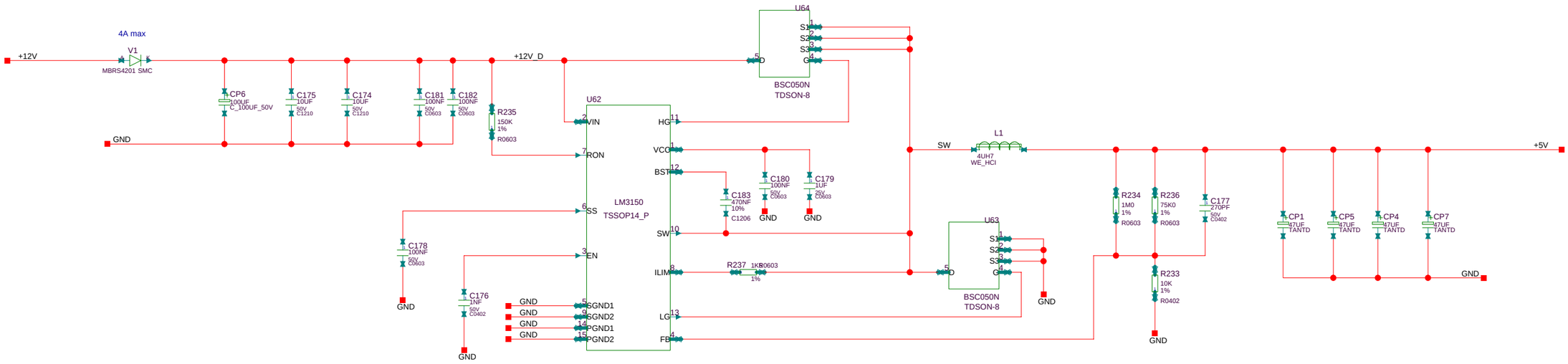
J23 GND GND
BANANE_LP180
B_35F234 / 236

J6 3 NC 2 1 GND +12V
AJ210B

J22 +12V +12V
BANANE_LP180
B_35F234 / 236







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A	B	C	D	E	F	G	H	I	J

7	6	5	4	3	2	1

U30

5SEEBH40C2N

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