# Designing with DSP Builder Advanced Blockset



### **Course Description**

Learn the timing-driven Simulink® design flow to implement high-speed DSP designs. This course focuses on implementing DSP algorithms using the advanced blockset capability of DSP Builder—an interface between Quartus® Prime software & MAT-LAB® and Simulink tools from The MathWorks. You'll analyze & design your DSP algorithm using the DSP Builder advanced blockset in MATLAB & Simulink. You'll explore architecture & performance tradeoffs with system-level constraints. Also you'll verify functionality & performance of generated hardware in the Quartus II software. Finally, you'll speed design time by incorporating ready made ModelIP cores in your design.

#### **Skills Developed**

- Implement DSP algorithms using Intel<sup>®</sup> DSP Builder Advanced Blockset
- Incorporate ModelIP and ModelPrim cores in a design
- Explore design architecture and performance tradeoffs using system level constraints
- Incorporate a DSP Builder Advanced Blockset model into a Qsys subsystem
- Verify the hardware performance and implementation in Quartus II software

#### **Skills Required**

- □ Familiarity with DSP fundamentals and design
- Familiarity with Intel Quartus Prime software is helpful, but not necessary
- Familiarity with Mathworks Matlab and Simulink is helpful, but not necessary
- Familiarity with digital modem design is helpful, but not necessary

#### Exercises

- Floating Point ModelPrim System
  - Implement a floating point ModelPrim System
  - Simulate the Design in Simulink
  - Verify the Design
  - Build Design in Quartus
  - Download and run the Desgin on a Board
- Algorithm Implementation using the ModelIP library
  - Calculate Theoretical Wire/Channel Structure of a DSP Algorithm
  - Build DSP algorithm using DSP Builder Advanced Blockset
- □ System Integration, Design Exploration
  - Incorporate a DSP Builder Advanced Blockset
    Component into a Qsys System and Quartus II
    Project
  - □ Explore Hardware Multiplier Trade-Offs

Course Length	1 day
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 800,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

## Intel<sup>®</sup> FPGA Technical Training

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