Introduction to the Platform Designer System Integration Tool

Course Description

This class will teach you how to quickly build designs for Intel® FPGA devices using the Platform Designer system-level integration tool (formerly known as Qsys), part of the Intel Quartus® Prime software. You will become proficient with using Platform Designer and learn how to quickly integrate "off-the-shelf" IP and custom logic into a system. Platform Designer makes design reuse easy through the use of standard interfaces, so you will learn about the interfaces supported by the tool: Avalon® Memory Mapped and Streaming as well as an introduction to the Arm* AMBA* AXI interface standard. The class provides a significant hands-on component, where you will gain exposure to tool usage as well as system and custom HDL component design.

Skills Developed

- Introduction to Platform Designer
  - What is Platform Designer (PD)?
  - Platform Designer user interface (UI)
  - Using Platform Designer in the FPGA design flow
  - Platform Designer files
- Platform Designer Interconnect
- Standard Interfaces & Signaling
- Off-the-shelf IP
- Creating custom components
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Skills Required

- Background in digital logic design
- Working knowledge of the Intel Quartus Prime software
- Knowledge of HDL coding methodology (helpful but not mandatory)

Exercises

- Introduction to Plaform Designer
  - Practice using the Platform Designer tool in the Intel Quartus Prime software's design flow
  - Investigate the Platform Designer's user interface
- Start Building a Video Datapath Hardware System Design
  - Build a datapath design in Platform Designer using components with Avalon®-MM and ST interfaces
  - Add a programmable state machine to the system to provide control over all the memory mapped slave ports of all the components in the system
- Complete and Test the System
  - Construct the required Avalon® interface for a custom logic block
  - Incorporate two custom components into the design using the Platform Designer Component Editor
  - Configure the state machine's Avalon-MM read and write accesses
  - Test the design in hardware

Course Length	1 day
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 800,- EUR / attendee
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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