Introduction to Verilog

Course Description

This class is a general introduction to the Verilog language and its use in logic design, covering the basic constructs used in both the simulation and synthesis environments. By the end of this course, you will have a basic understanding of the Verilog module, data types, operators and assignment statements needed to begin creating your own designs, using both behavioral and structural approaches. In the hands-on laboratory sessions, you will get to practice the knowledge you have gained by writing simple but practical designs. You will check your designs by compiling in the Quartus® Prime software version and simulating in the ModelSim® - Intel® tool.

Skills Developed

- Create a basic Verilog module
- Understand the difference between simulation and synthesis environments
- Understand Verilog data types and operators and their uses
- Model hardware and test using behavioral modeling constructs
- Model hardware and test using structural modeling constructs

Skills Required

- Background in digital logic design
- Knowledge of simulation is a plus
- Prior knowledge of a programming language (e.g., "C" language) is helpful, but not required
- No prior knowledge of Verilog HDL or Quartus Prime software is needed

Exercises

- Build a 16-bit adder
- Build a 4x4 multiplier
- Build a 4-bit 2:1 multiplexer
- Build an 8-bit to 16-bit shifter
- Build a 7-segment display using CASE statement
- Build a 16-bit register with synchronous operation
- Build a 2 bit counter with asynchronous operation
- Examine the controlling state machine
- Putting it all together by declaring and instantiating the lower-level components

Course Length	1 day
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 800,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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