Mastering Timing Analysis and Timing Closure in Intel FPGAs

Course Description

Building upon your basic understanding of creating Synopsys Design Constraint (SDC) timing constraints, this class will guide you towards understanding, in more depth, timing analysis and timing closure. Examples include thoroughly analyzing the design for timing failures, adjusting settings and assignments according to tool recommendations, selecting correct clock resources and writing HDL code for optimal performance.

Agenda

- Timing Analysis Fundamentals
  - Terms and Definitions
  - Arrival and Required Times
  - Slack Calculation
- SDC Basics Review
  - Collections
  - Clock Constraints
  - I/O Constraints
  - Timing Exceptions
  - Clock enable multicycle exceptions
- Using Tcl with Timing Analysis
- SDC and Tcl Examples
- Timing Reports Review
- Timing Failure Analysis Flow
  - Check Compiler Results
  - Check Timing Constraints
  - Follow Tool Recommendations
    - Adjust Tool Settings
  - Recompile & Generate Detailed Timing
  - Reports
  - Evaluate Results
- Chip Planner
- Analyzing and Solving Timing Failures
  - Too many logic levels
  - High fanout
  - Conflicting physical constraints
  - Tight timing
  - Clock crossing
  - Clock skew
- The Fitter, Seeds and Design Space Explorer
- Understanding Device Clocking Resources
  - Hierarchical clocking resources
  - Clock control blocks
  - Utilizing global routing resources
- Additional Timing Closure Topics
  - Rapid Recompile
  - Close timing through over-constraining
  - Incremental Compilation Timing Closure Methodologies
- Timing Closure in Qsys Systems

Skills Required

- Some working knowledge of the TimeQuest timing analyzer and basic SDC commands
- Background in digital logic design
- Experience with PCs and the Windows operating system

Exercises

- Multicycle Constraints for Clock-Enabled Designs
- Timing Analysis and Tcl
- Analyze and Fix Basic Timing Failures
- Practice Fixing Other Timing Failures
- Timing Optimization using PLLs

Course Length	2 days
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 1550,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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