Performance Optimization with Stratix® 10 HyperFlex® Architecture

Course Description

In the Performance Optimization with Stratix 10 HyperFlex Architecture course, you will learn Quartus® Prime software features and some basic design techniques that will enable your designs to take advantage of the Stratix 10 HyperFlex architecture. In the training, you will learn two steps to improving your performance with the HyperFlex architecture, namely Hyper-Retiming and Hyper-Pipelining, with each step allowing you to move your design up the performance curve.
Note: While the focus of this course is the Stratix 10 device family, many of the techniques you will learn can be used to improve performance in other device architectures.

Skills Developed

- Describe the Stratix 10 device architecture, including the new HyperFlex architecture
- Enable the Quartus software features that take advantage of the HyperFlex architecture
- Evaluate possible design improvements using the Quartus software's Fast Forward Compile feature
- Improve your Stratix 10 design performance by understanding and enabling Hyper-Retiming
- Improve your Stratix 10 design performance by implementing zero-latency Hyper-Pipelining

Skills Required

- Familiarity with FPGA/CPLD design flow
- Familiarity with the Quartus design software
- Familiarity with Verilog or VHDL synthesizable design structures

Exercises

- Fast Forward Compile
  - Run Fast Forward Compile
  - Examine the Fast Forward Compile reports
  - Explore different Fast Forward Compile options
- Hyper-Retiming
  - Analyze Hyper-Retimer report recommendations on removing asynchronous clears
  - Edit a design to remove asynchronous clears and see the results
- Hyper-Pipelining
  - Read Fast Forward Compile reports
  - Add registers where indicated by reports
  - Verify functionality with simulation
  - Verify performance with Fast Forward Compile turned off

Course Length	1 day
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 800,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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