Quartus® Prime Foundation Workshop



Course Description

This workshop gives a comprehensive introduction into designing with Intel® FPGA design software and Intel programmable logic devices. It is suitable for en-gineers who are new to programmable logic design or who have already designed some logic and would like to gain a deeper understanding of the design flow, the available tools and how to control specific device fea-tures. The workshop is a combination of lectures and hands-on exercises.

Agenda

- Understand programmable logic architectures
- □ Understand the programmable logic design flow
- Learn golden design rules for programmable logic
- Manage Quartus Prime projects
- Work with different design entry options
 - Schematic design entry
 - HDL design entry
 - □ IP Catalog
 - Platform Designer (fka Qsys)
- Simulate a design with ModelSim
- Plan & manage device I/O assignments using Pin Planner
- Analyze clock & input/output timing using
- 🗆 TimeQuest
- Review compilation results
- Work with Debugging Tools
 - Sources & Probes
 - 🗆 SignalTap

Skills Required

- Background in digital logic design
- Experience with PCs and the Windows operating system

Exercises

- □ Create a project using the New Project Wizard
- Design Entry
- Compilation
- Revisions and Assignments
- □ I/O Assignments
- Timing Assignments
- PlatformDesigner (Qsys)
- Simulation with ModelSim
- Debugging with In-System Sources & Probes and SignalTap II

Course Length	3 days
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 2250,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel[®] FPGA Technical Training

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