Quartus® Prime Design Series
Timing Analysis

Course Description

You will learn how to constrain & analyze a design for timing using the TimeQuest timing analyzer in the Quartus Prime software. This includes understanding FPGA timing parameters, writing Synopsys Design Constraint (SDC) files, generating various timing reports in the TimeQuest timing analyzer & applying this knowledge to an FPGA design. Besides learning the basic requirements to ensure that your design meets timing, you will see how the TimeQuest timing analyzer makes it easy to create timing constraints to help you meet those requirements.

Skills Developed

- Understand the TimeQuest timing analyzer timing analysis design flow
- Apply basic and complex timing constraints to an FPGA design
- Analyze an FPGA design for timing using the TimeQuest timing analyzer
- Write and manipulate SDC files for analysis and controlling the Quartus II compilation

Prerequisites

We recommend completing one of the following courses:

- The Quartus Prime Software Design Series: Foundation (Instructor-led Training)
- The Quartus Prime Software Design Series: Foundation (Online Training)

Skills Required

- Experience with PCs and the Windows operating system

Exercises

- Introduction to the TimeQuest Tool
- Clock Constraints
- Synchronous I/O Constraints
- Timing Exceptions & Analysis

Course Length	1 day
Language	Presentation in German or English and documentation in English
Platform	PC Windows 10
Pricing	Public: 800,- EUR / attendee In-House: On Request
Dates	See schedule at elcamino.de

Intel® FPGA Technical Training

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