Advanced Timing Analysis with TimeQuest

El Camino
Training - Engineering - Consultancy

Course Description

You will improve your proficiency in writing Synopsys Design Constraint (SDC) files and performing timing analysis using the TimeQuest timing analyzer. You will write SDC files to constrain the more advanced types of interfaces and blocks used in today's FPGA designs. You will then analyze these designs to verify proper operation and performance. You will also learn how to automate the process of constraining and analysis by writing customized Tcl script files.

Skills Developed

- Write Tcl script files to automate constraining and analysis of FPGA designs
- Apply timing exceptions to real design situations
- Properly constrain and analyze the following design situations
  - Source synchronous interfaces
  - External feedback designs
  - High-speed interfaces containing dedicated SERDES hardware

Skills Required

- Experience with PCs and the Windows operating system
- Completion of The Quartus Prime Software Design Series: Timing Analysis course OR a working knowledge of the TimeQuest timing analyzer and basic SDC commands

Course Length	2 days
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows 7 or Windows 10
Pricing	Public: see www.elcamino.de Individual: on request
Dates	Public: see www.elcamino.de Individual: on request

Exercises

- Timing Analysis and Tcl
- Multicycle Constraints for Clock-Enabled Designs
- Source Synchronous Interfaces – Single Data Rate
- Source Synchronous Interfaces – Double Data Rate
- Constraining Feedback Designs
- LVDS Timing Analysis

El Camino GmbH
Landshuter Str. 1
84048 Mainburg
Germany

phone: +49-8751-8787-0
fax: +49-8751-8787-10
e-mail: info@elca.de
www.elcamino.de