Course Description
In this course, you will learn & practice efficient coding techniques for VHDL synthesis. You will gain experience writing behavioral & structural code & learn to effectively code common logic functions including registers, memory & arithmetic functions. You will use VHDL constructs to parameterize your designs to increase their flexibility and reusability. While the concepts presented will mainly be targeting Altera® devices using the Quartus® II software environment, many can be applied to synthesizing hardware using other synthesis tools as well. You will also be introduced to testbenches, VHDL constructs used to build them & common ways to write them. The hands-on exercises will use Quartus II software to process VHDL code and ModelSim®-Altera software for simulation.

Skills Developed
- Develop coding styles for efficient synthesis when:
  - Targeting device features
  - Inferring logic functions
  - Using arithmetic operators
  - Writing state machines
  - Use Quartus II software RTL Viewer to verify correct synthesis results
  - Incorporate Altera structural blocks in VHDL designs
  - Write simple testbenches for verification
  - Create parameterized designs

Prerequisites
We recommend completing the following courses:
- Introduction to VHDL
- VHDL Basics

Skills Required
- Completion of the "Introduction to VHDL" course or some prior knowledge and use of VHDL
- Background in digital logic design
- Understanding of synthesis and simulation processes