VHDL Workshop

El Camino
Training - Engineering - Consultancy

Course Description

This three-day class is a general introduction to the VHDL language and its use in programmable logic design. The emphasis is on the synthesis constructs of VHDL. You will gain a basic understanding of VHDL, enabling you to create your own designs. In the hands-on laboratory sessions, you will put this knowledge to the test by writing simple but practical code. You will also learn the basic instructions needed for operating the synthesis and simulation tools Quartus Prime. Furthermore the implementation of test benches and the use of ModelSim for VHDL simulation will be covered.

Skills Developed

- Understanding the origin of the VHDL language
- Understanding the language basics
- Using VHDL building blocks (Design Units)
  - Entity
  - Architecture
  - Configurations
  - Package declarations
  - Package bodies
- Ability to model code styles
  - Behavioral code style
  - Structural code style
- Understanding the design methodologies of VHDL and the differences in Synthesis models
- Using VHDL for simulation
- Working with ModelSim to perform both functional and gate level simulations

Skills Required

- Background in digital logic design
- Prior, basic knowledge of a programming language or hardware description language is a plus
- No prior knowledge of VHDL, Quartus Prime or ModelSim software is needed.

Course Length	3 days
Language	Presentation in German or English Slides and documentation in English
Platform	PC Windows 7 or Windows 10
Pricing	Public 1500,- EUR/attendee In-House On Request
Dates	See schedule at http: //www.elcamino.de

Exercises

- Implementing a 16-bit adder using the + operator
- Build a four input 2:1 multiplexer using IF-THEN statement
- Build a 7-segment display using CASE statement
- Build an 8-bit to 16-bit shifter using a FOR LOOP statement
- Build a 16-bit register with synchronous operation
- Build a 2 bit counter with asynchronous operation
- Examine a controlling state machine
- Build a 4x4 multiplier using LPM_MULT
- Putting it all together by declaring and instantiating the lower-level components
- Basic Simulation with ModelSim-Intel FPGA Edition
- Simulating with Altera Megafunctions
- How to use IF-THEN efficiently
- Structural Design by Instantiating MegaWizard® Components
- Operator Balancing & Resource Sharing
- Create a VHDL test bench
- Writing Parameterized Code

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